PARTIAL RESPONSE SIGNALLING USING TRANSLINEAR CIRCUITS FOR BASE BAND DIGITAL COMMUNICATION SYSTEMS

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by
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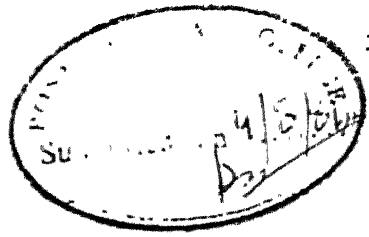
to the

DEPARTMENT OF ELECTRICAL ENGINEERING



CERTIFICATE

Certified that this work 'PARTIAL RESPONSE SIGNALLING USING TRANSLINEAR CIRCUITS FOR BASEBAND DIGITAL COMMUNICATION SYSTEMS' by Capt. N.V. Pande has been carried out under my supervision and has not been submitted elsewhere for a degree.

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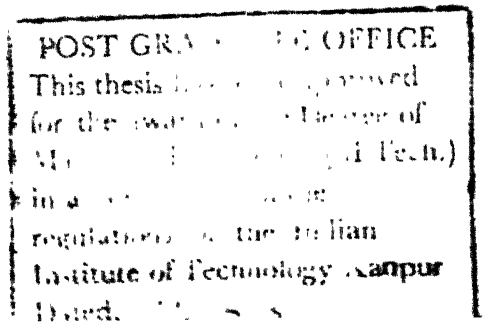

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- Capt. N.V. Pande

ABSTRACT

Partial Response Signalling, also known as correlative encoding uses finite amount of Intersymbol Interference (ISI) as against the zero memory systems. They utilize the spectral bandwidth more efficiently and are able to achieve the Nyquist rates or more, over restricted Nyquist-bandwidth. Normally these schemes require critical and difficult to design filters.

In this thesis the correlative encoding is achieved by nonlinear wave shaping as against the conventional filter. The method is easy to design, implement and gives good results in terms of eye openings, spectral power content, out of band rejection and bit-error rate. In addition the system is modular and can be used for any PRS polynomial.

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CHAPTER 1

REVIEW OF ZERO MEMORY SYSTEMS AND CONCEPT OF CORRELATIVE CODING

1.1 INTRODUCTION:

Conventionally baseband digital data transmission is done by bandlimiting the data stream by a low pass filter and sending the resulting signal over a bandlimited channel. If one uses a rectangular ideal low pass filter and Nyquist rate, a transmission efficiency of 2 bits/sec/Hz can be achieved. Such a scheme avoids intersymbol interference (ISI) but is difficult to realize and is very sensitive to timing perturbations at the receiver. Raised cosine class of filters can be used which require extra bandwidth or in other words can operate at lower data rates. Multilevel transmission systems can be used but they need extra circuitary and are more susceptible to noise as compared to two level transmission.

Correlative encoding, first suggested by A. Lender [1] and later generalised by Kretzmer [2] utilizes controlled ISI generated at the transmitting end. These encoding schemes, also known as Partial response signalling (PRS) utilize the frequency spectrum better than the zero memory systems.

Number of PRS schemes exist like Duobinary and Modified duobinary (MDB). These permit txn at 2 bits/sec/Hz rate, have lower sensitivity to timing error and can monitor the error condition in the channel.

The design of the low pass filter is crucial to the error performance of these schemes. An alternative method of non-linear waveshaping to produce the desired pulse shape was suggested by Feher [4] using analog switches to gate in or out suitably phased triangular or sinusoidal waveforms. However the scheme can not be used at high data rates due to limitations of analog switches.

In this work the nonlinear waveshaping concept is extended to much higher data rates by using Gilbert cells or the bipolar transistor version of the double balanced four quadrant modulator/demodulator. A single MDB transmission filter can be designed with two Gilbert cells. The technique can be easily extended to any other PRS polynomial. It can be driven with ECL or TTL logic and exploits the non-saturating current steering and commutation capabilities of the Gilbert-cells. The overall scheme gives good eye patterns and is capable of operating in Megabits range.

1.2 THE ZERO MEMORY SYSTEMS:

The block diagram of a synchronous data transmission channel is shown in Fig. 1.1.

Consider that data pulse train at 1/T pulses/sec is being transmitted on the channel. The pulse spacing is T seconds.

The channel shapes these pulses, producing pulses of considerable tails . In an ideal case the pulse when shaped by the overall channel (consisting of Tx and Rx filters and the channel), should be restricted to its own time slot so that the detector can independently detect it. This would be zero memory system. However the overall channel transfer function is such that the tails of each pulse overlap into the time slot of the next pulse. This interference (inter-symbol interference or ISI) can cause error in detection even in the absence of noise. So we consider those channel transfer functions in which the ISI is eliminated.

1.2.1 Pulse Shape for Zero ISI:

Nyquist considered the problem of designing the transfer function g(t) such that the ISI at sampling instances is eliminated. Nyquist showed that for a data rate of 1/T bits/sec, a bandwidth of $\frac{1}{2T}$ Hz is sufficient.

If we consider the data pulses to be ideal rectangular pulses, to retain their shape the channel would be required to be able to pass infinite frequency content. This is uneconomical. The channel is always bandlimited. Also it

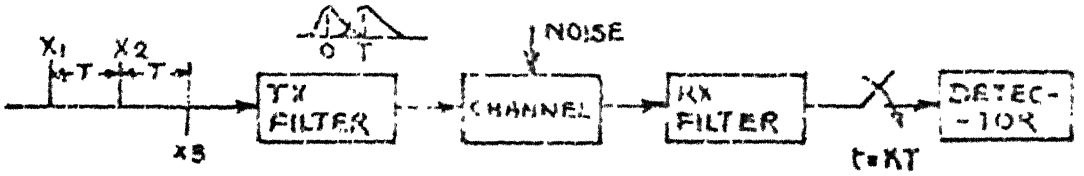


Figure. 1·1 : Synchronous Transmission System

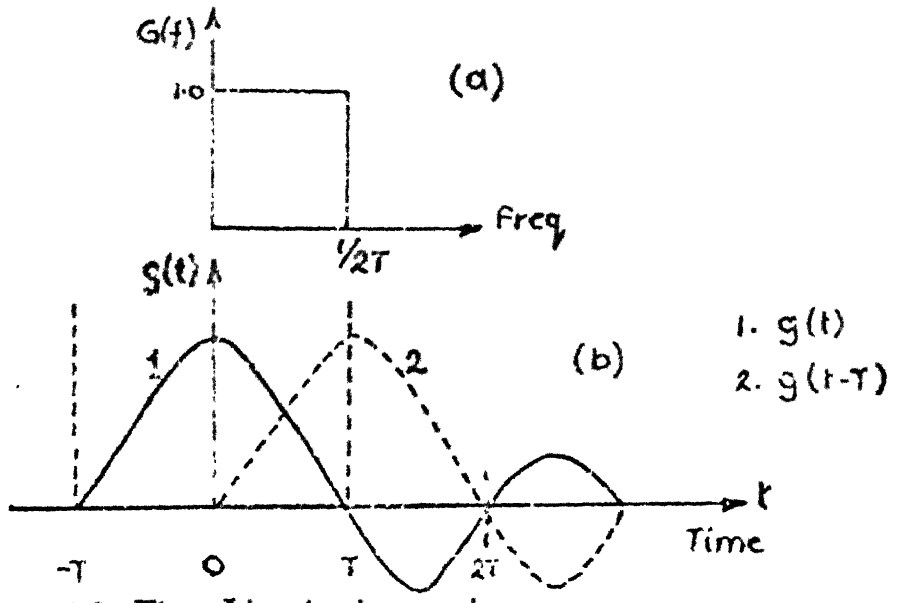
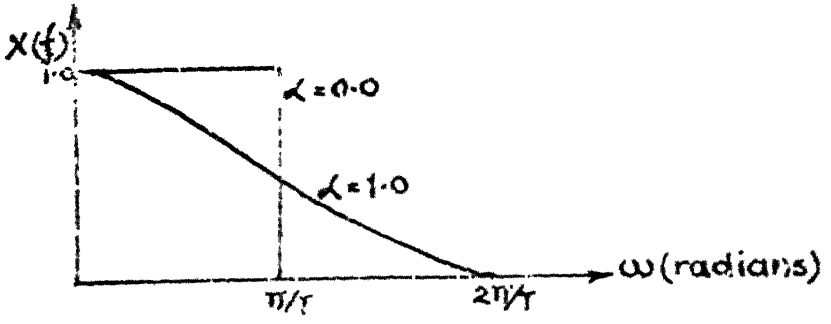


Figure. 1·2 : The Ideal channel



would be desirable to exclude components of noise and interference outside the band having maximum signal energy. As such we want the channel to have low pass characteristics. The equivalent channel for minimum bandwidth then, should have transfer function as shown in Fig. 1.2(a).

The corresponding time response is shown in Fig. 1.2(b). The cut-off frequency is $\frac{1}{2T}$ Hz and is known as Nyquist bandwidth for Nyquist data rate of $\frac{1}{T}$ symbols/sec.

As shown in Fig. 1.2(b), g(t) has a long tail ending at infinity and it passes through zero at all other sampling instances, causing no ISI to other pulses. Each symbol can then be detected without any error independently without any knowledge about the previous bit (zero memory).

The bandwidth requirement for ISI free detection given by Nyquist is based on certain assumptions known as Nyquists criteria.

a) <u>The first criterion</u>: To achieve the Nyquist rate in Nyquist bandwidth there is to be no ISI at the sampling instances. The channel with transfer function as shown in Fig. 1.2 fulfills this requirement. Although it is impractical to design such a brick wall filter, if we assume it to be approximated with infinite delays, there is another drawback. The time response of this channel is seen to be very slowly

dying $\frac{\sin(x)}{x}$ function. So although it passes through zero at every sampling instance ideally, any slight deviation in the sampling instant or any slight deviation of bit rate causes large ISI. That is, the system can not tolerate any timing perturbations at all and is impractical.

b) The Second Criterion: Nyquists second criterion is that there is no ISI at transition instances or rather at half way points between adjacent signal pulses. This requires filter with frequency response as cos $\omega T/2$ with cutoff frequency at 1/2T Hz. However now signalling at 1/T bits/sec is not possible as the filter will not pass the frequency 1/2T Hz and thus a steady alternating pattern 10101010... at the rate 1/T bit/sec with fundamental frequency 1/2T Hz can not be transmitted through the filter satisfying the Nyquists second criterion.

Thus it is seen that for zero memory systems it is impractical to achieve the Nyquist rate in minimum bandwidth channels.

1.2.2 Channels Using Extra Bandwidth:

One way to achieve the Nyquist rate is by increasing the bandwidth.

The first criterion of Nyquist of no ISI at sampling instances remains satisfied if we add a function odd about

1/2T Hz to the rectangular filter. Similarly the second criterion is still satisfied if a function even about the cutoff frequency (1/2T) of the required cos πT/2 filter is added. Both these variations need extra bandwidth.

A filter shape which satisfies both the above mentioned conditions is the well known 'Raised cosine filter'. The transfer function for this is given below in (1.1) and is shown in Fig. 1.3.

$$X(\omega) = \begin{cases} T & \text{for} \quad 0 \leq \omega \leq \pi/T(1-\alpha) \\ T/2[1-\sin(\frac{T}{2\alpha}(\omega - \frac{\pi}{T}))] & \pi/T(1-\alpha) \leq \omega \leq \pi/T(1+\alpha) \end{cases} \qquad (1.1)$$

where $\alpha = \frac{\text{Excess bandwidth}}{\text{Nyquist bandwidth}}$.

So we can reach Nyquist's rate but only at the cost of extra bandwidth.

1.2.3 Multilevel Systems:

Another method to achieve Nyquist rate is by multilevel transmission. M levels are transmitted (M=2 for normal binary transmission). The number of levels M is power of two i.e. $M=2^K$ where K is a +ve integer. So K=1 for binary and each level represents K bits of information. Consider 4 levels being transmitted (K=2). So each level can carry two bits of information viz. 00, 01, 10 and 11 for M=4. Thus for M-aray transmission we have K bits/sec/Hz which is K times the data rate of binary.

Although the multilevel systems can achieve these higher data rates, these are complex and are more

sensitive to noise. Since now one out of 4 levels has to be detected, small noise can cause wrong level detection.

1.3 THE PARTIAL RESPONSE SIGNALLING:

As against the zero memory system which tries to eliminate ISI at sampling instances the partial response systems first introduced by A. Lender [1] and subsequently generalized by Kretzmer [2], use controlled amount of ISI.

Partial Response Signalling (PRS) also known as correlative coding, deliberately introduces a limited amount of ISI over a span of one, two or more digits thus causing spectral reshaping. As a result, for a given bandwidth and power input to the channel, PRS permits transmission of more bits/sec/Hz than zero memory for the same error rate. Nyquist and higher rates are possible. Due to the correlation between digits the pulse train has distinct patterns which can monitor error conditions of the channel.

These controlled ISI added signals are then interpreted accordingly at the receiver.

The transfer function of such correlative systems (Trans and Receive) has the following form,

$$F(\omega) = \sum_{K=0}^{n} a_K \, e^{-jK\omega T}$$

where $a_0 = 1$ and $a_K = +1$ or 0

1.4 OUTLINE OF THE THESIS:

Normally the correlative coding is implemented by use of critical analog filters. In this work these schemes have been implemented using nonlinear waveshaping. In this chapter the zero memory systems and their limitations have been reviewed and the need for PRS systems is brought out.

In Chapter 2 the Partial Response schemes are reviewed alongwith their conventional implementation. Feher [4] suggested a method of pulse overlapping for ISI free transmission which is then reviewed alongwith its limitations.

In Chapter 3 the trans-linear wave-shaping circuit used for realizing the PRS is discussed. The actual implementation details for Modified Duobinary (MDB) are given and it is explained as to how this can be extended to any other PRS polynomial.

Chapter 4 deals with the performance of the translinear implementation and various measurements.

We conclude in Chapter 5 with some suggestions for further scope of work in this topic.

CHAPTER 2

PARTIAL RESPONSE SIGNALLING

The limitations of the zero memory systems were discussed in the previous chapter. The zero memory systems try to eliminate the ISI. As against ... the partial response signalling (PRS) introduces deliberately the ISI due to previous bits in controlled quantity. This causes spectral reshaping viz. placing nulls in the frequency response. The system thus can accept timing jitter and can reach Nyquist rate.

PRS was first introduced by Lender [1] and then generalized by Kretzmer [2]. A lot of work has since been done on the subject, the details of which can be found in the unified study paper by Kabal and Pasupathy [3] and the paper by Kobayashi [5].

In this chapter we will discuss the PRS, its advantages, performance and implementation.

2.1 THE GENERALIZED PRS SYSTEM:

We consider the ideal system with no imperfections in the channel. Suppose the overall transfer function is $H(\omega)$ including the TX and RX filters and the channel. The ideal system has impulse response $h(t)$. Let N be the smallest

number of continuous samples that span all nonzero samples. Then if $\{fn\}$, n = 0,1,2,...,N-1 are these N sample values, the PRS system polynomial is

$$F(D) = \sum_{n=o}^{N-1} fn\ D^n \tag{2.1}$$

where D is the delay operator.

For input sequence $\{x_n\}$ the output sequence $\{y_n\}$ is given by

$$Y(D) = X(D)\ F(D) \tag{2.2}$$

where,

$$Y(D) = \sum_{n=o}^{\infty} Y_n D^n \tag{2.3}$$

The $\{x_n\}$ will be assumed to be independent m-ary symbols taking equally likely values -(m-1), -(m-3),..., (m-3), (m-1)

Fig. 2.1 shows a method of generating the PRS system function $H(\omega)$. The system consists of a delay line with coefficients 'fn'. The added signal passes through a filter with frequency response $G(\omega)$. The transversal filter has the periodic frequency response of period $2\pi/T$ given as

$$F(\omega) = F(D)\Big|\ D = \exp(-j\omega T) \tag{2.4}$$

$$= \sum_{n=o}^{N-1} fn\ \exp(-j\omega nT) \tag{2.5}$$

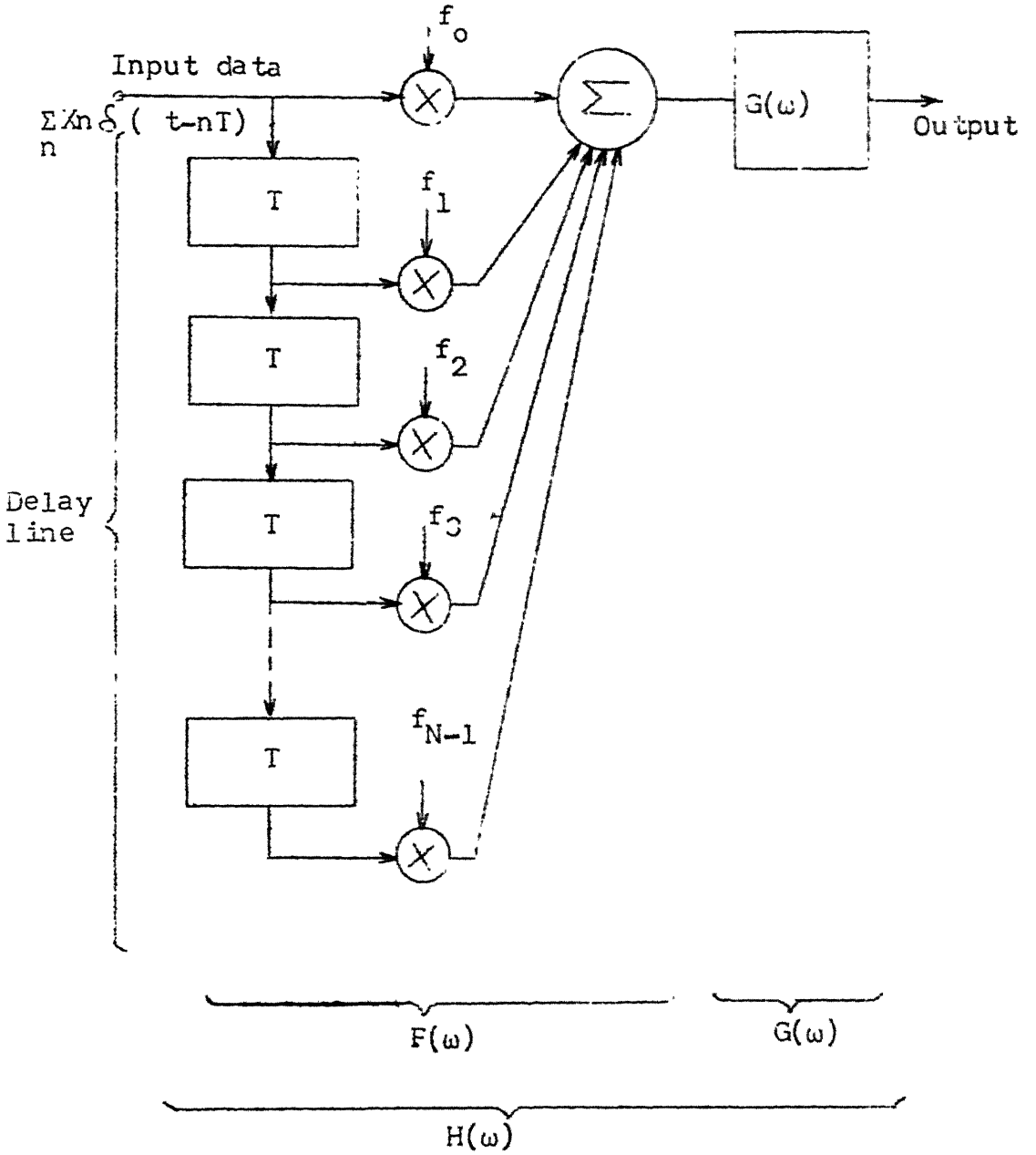


Figure 2.1: Generalized partial response signalling

where T is the symbol spacing.

It can be shown that h(t) has sample values $\{f_n\}$ iff. $G(\omega)$ satisfies Nyquist's first criterion.[7]

The PRS system shown above is divided into two parts. $F(\omega)$ forces the desired sample values but is periodic, $G(\omega)$ preserves the sample values but can be used to bandlimit the channel. For actual implementation this seperation may not exist.

Based on the generalized PRS diagram of Fig. 2.1, a number of PRS polynomials can be chosen by choice of $\{f_n\}$ and by choice of $G(\omega)$.

2.1.1 The Choice of PRS Polynomial:

Some of the considerations for choosing the PRS polynomial are given below.

a) Bandwidth of the channel: To maximise data rate in available bandwidth, many PRS systems are designed to occupy minimum Nyquist bandwidth. That means the transfer function $G(\omega)$, of the Fig. 2.1 is chosen as an ideal rectangular filter. Other choices of $G(\omega)$ occupying larger bandwidth can be used provided data rate and bandwidth are not important considerations. The implementation of ideal Nyqyist filter need not bother us here since the overall

filter to be implemented is a combination of the delays and the brick wall filter.

b) Spectrum nulls: The addition of ISI reshapes the frequency spectrum. Thus we can choose the filter to insert spectral nulls at chosen points.

Spectral null at zero frequency (DC) can be useful for transformer coupled circuit, dc powered cables, SSB modem etc.

Similarly other spectral null say at frequency $\frac{1}{2T}$ can be useful for inserting pilot tones at these frequencies.

c) Output levels: The basic concept of PRS is the mapping of the input data levels into more levels based on certain rules. As such the number of output levels is an important consideration for choosing the system polynomial.

The number of output levels for correlative system is a compromise between complexity of the circuit and the data rate viz-a-viz the error rate performance.

The PRS system with M nonzero pulse samples will have m^M output levels for m-ary input unless there are special relationships between the sample values. The number of output levels L lies in the range

$$M(m-1) + 1 \leq L \leq m^M \qquad (2.6)$$

with the minimum value being obtained when the pulse samples have the same magnitude.

Kabal and Pasupathy [3] have given a detailed reasoning in choosing the PRS polynomials and have shown that (1-D) and (1+D) being factors of the polynomials have certain specific advantages. Two of the most popular schemes are discussed in the next section. The various partial response systems formed with (1-D) and (1+D), as factors alongwith their details are attached at Appendix 'A'.

2.2 DUOBINARY AND MODIFIED DUOBINARY PRS SCHEMES:

Duobinary and Modified duobinary are two popular PRS schemes. These are discussed in detail below.

2.2.1 Duobinary Signalling:

The duobinary signalling is characterized by system polynomial (1+D). The filter for this is shown in Fig. 2.2.

Duobinary implies doubling the speed of binary. Consider a binary data train at input (A) in Fig. 2.2, represented by impulses $\pm\delta(t)$. The output at (B) in Fig. 2.2 is $(\delta(t) + \delta(t-T))$ with +ve or -ve appropriate sign.

Then

$$h_1(t) = \mathcal{F}^{-1}\,(H_1(f))$$

$$= \delta(t) + \delta(t-T) \qquad (2.7)$$

where T is bit interval.

So,

$$H_1(f) = \mathcal{F}(h_1(t))$$

$$= 1 + e^{-j2\pi fT} \tag{2.8}$$

$$= 2 \cos \pi fT \tag{2.9}$$

To limit the bandwidth the Nyquist filter $H_2(f)$ is used such that

$$H_2(f) = \begin{cases} T & |f| \leq 1/2T \\ 0 & \text{elsewhere} \end{cases} \tag{2.10}$$

The overall transfer function of the duobinary filter H(f) is given by

$$|H(f)| = |H_1(f)| . |H_2(f)| \tag{2.11}$$

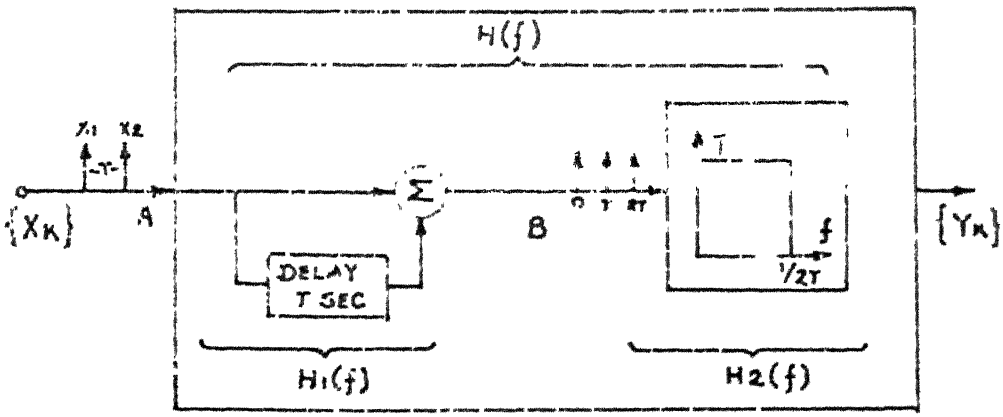
$$= \begin{cases} 2T\cos \pi fT & |f| \leq \frac{1}{2T} \\ 0 & \text{elsewhere} \end{cases} \tag{2.12}$$

The frequency response is shown in Fig. 2.3 for the two parts $H_1(f)$ and $H_2(f)$ and for combined overall duobinary filter.

The impulse response of the duobinary filter H(f) obtained from (2.12) is given by

$$h(t) = \frac{\sin \pi t/T}{\pi t/T} + \frac{\sin \frac{\pi(t-T)}{T}}{\frac{\pi(t-T)}{T}} \tag{2.13}$$

This is shown in Fig. 2.4.



T = Bit duration

Figure. 2.2 : Duobinary Filter

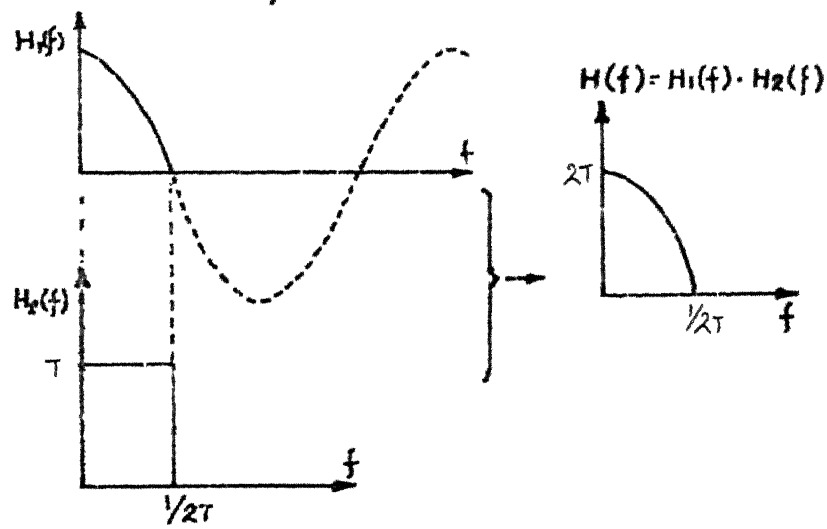


Figure. 2·3 · Duobinary Filter Response

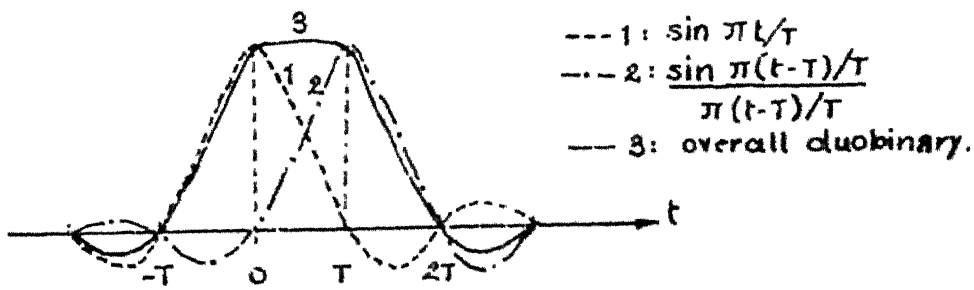


Figure. 2·4 : Duobinary Impulse Response.

It shows that if 1 and -1 represent the two binary states at the input, the output levels will be +2 for a 1 following a 1, 0 for 1 following 0 or vise-versa and -2 for 0 following a 0 (That is considering +1 for 1 and -1 for a zero). So at sampling instance there will be three levels ± 2 and 0 to be detected and not two. So we have 3 levels and bandwidth is still Nyquist and Nyquist rate or upto 43% higher can be achieved [7].

Referring to Fig. 2.2 if the input x_K is ± 1, the output y_K will be ± 2 or 0.

$$Y_k = X_K + X_{K-1}$$

For detecting to get x_K again we have $\hat{X}_K = Y_K - Y_{K-1}$

Thus we see that if any error is made in detecting a bit the next and the next ... bit detection will be wrong. This phenomenon is known as error propagation. To counter this we resort to precoding.

2.2.1.1 Precoding for Duobinary:

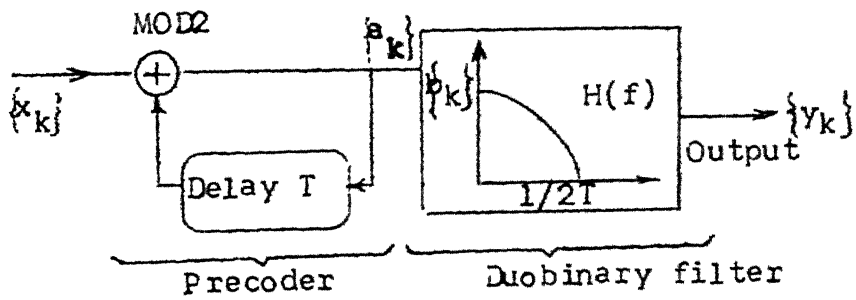


Fig. 2.5: Precoding for duobinary

The precoding used to avoid error propogation is the nonlinear operation shown in Fig. 2.5. The input data sequence $\{x_K\}$ is converted into a sequence $\{a_K\}$ by the rule

$$a_K = x_K \oplus a_{K-1}$$

where $\oplus$ is modulo 2 addition.

It then passes through the duobinary filter. The effect of the precoding is explained in Table 2.1.

Table 2.1

x_K		0	0	1	0	1	1	0	1	
a_K $(a_K = x_K \oplus a_{K-1})$	0	0	0	1	1	0	1	1	0	$\oplus$ Mod 2
b_K $(b_K = 2a_K - 1)$		-1	-1	1	1	-1	1	1	-1	
y_K			-2	0	2	0	0	2	0	
$\hat{x}_K = y_K \pmod 2$			0	1	0	1	1	0	1	

Now the output y_K is ± 2 for zero of the original data and 0 for one of original data. The decision (y_K mod 2) is independent of any past bit and error propogation is avoided.

2.2.2 Modified Duobinary (MDB):

Another popular scheme used is the modified duobinary (MDB). The system is characterized by polynomial $(1-D^2)$ where D^2 is delay of 2 bit durations. The implementation is shown in Fig. 2.6.

Now $h_1(t)$ is given as

$$h_1(t) = \delta(t) - \delta(t-2T) \tag{2.14}$$

so, $$H_1(f) = 1-e^{-j4\pi fT}$$

$$= 2 \sin 2\pi fT \tag{2.15}$$

and $$H_2(f) = \begin{cases} T & \text{for } f \leq 1/2T \\ 0 & \text{elsewhere} \end{cases} \tag{2.16}$$

and the overall MDB transfer function is given as

$$|H(f)| = |H_1(f)| \cdot |H_2(f)| \tag{2.17}$$

$$= \begin{cases} 2T \sin 2\pi fT & \text{for } |f| \leq 1/2T \\ 0 & \text{elsewhere} \end{cases} \tag{2.18}$$

This is shown in Fig. 2.7. Equation (2.15) can be written as

$$H_1(f) = (1-e^{-j2\pi fT}) \cdot (1+e^{-j2\pi fT}) \tag{2.19}$$

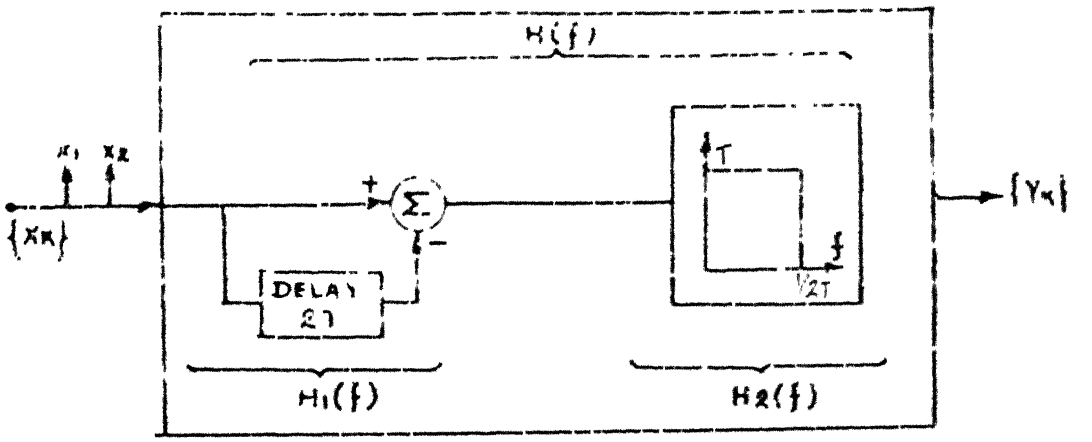


Figure. 2·6 : Modified duobinary filter.

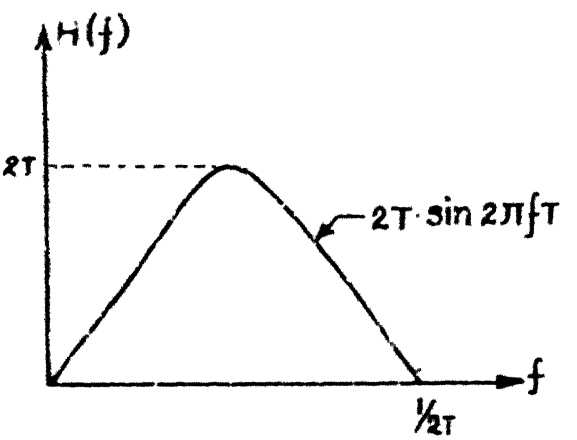


Figure. 2·7 : MDB filter respnse.

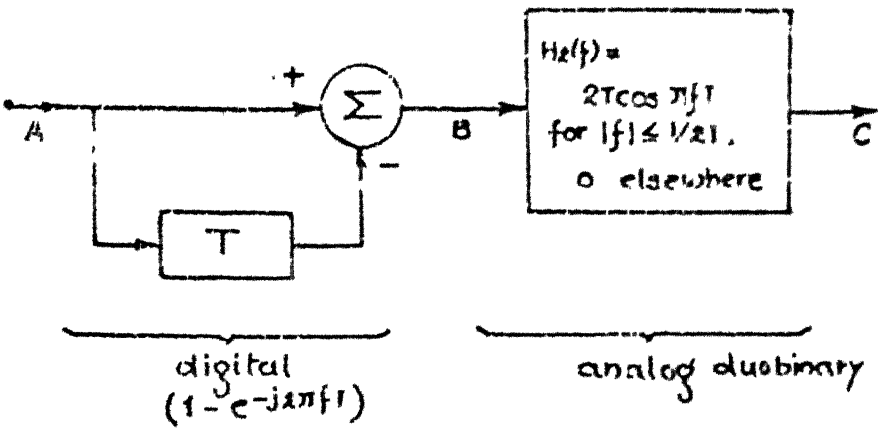


Figure. 2·8 : MDB Implementation.

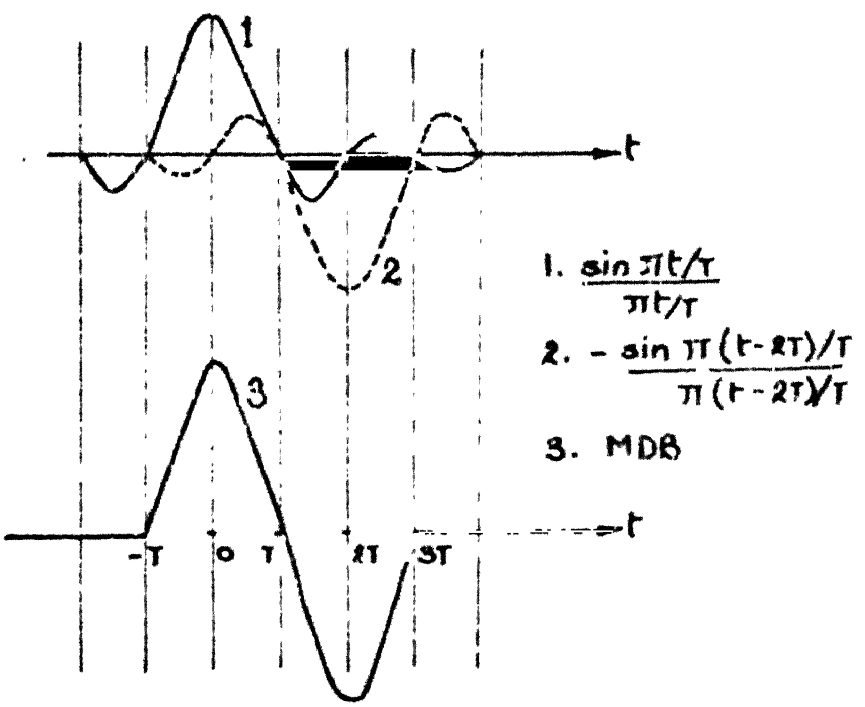


Figure. 2·9 : MDB Impulse response.

Now it can be seen that if we combine the second bracket in (2.18) along with the $H_2(f)$, the filter is the same as the duobinary filter of the previous section and the first bracket of (2.18) can be digitally implemented. This scheme of implementation is shown in Fig. 2.8.

The impulse response for MDB $(1-D^2)$ is shown in Fig. 2.9.

The present bit will cause ISI for the bit next to the next bit and for correct detection we have to substract it. So error propogation can occur if a bit is wrongly detected. We again resort to precoding which is shown in Fig. 2.10.

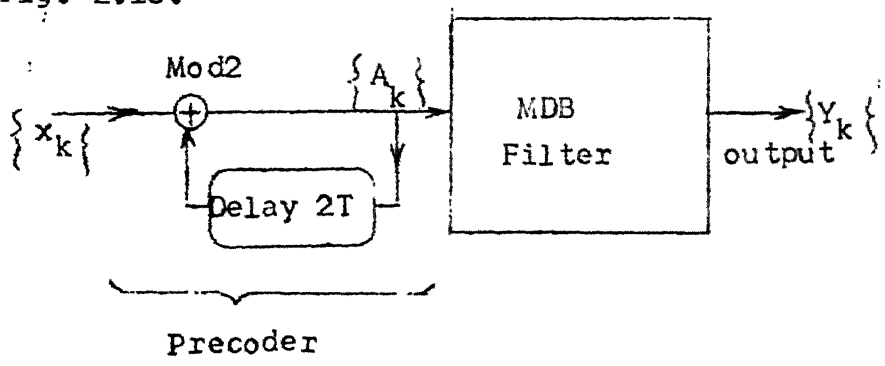


Fig. 2.10: MDB Precoding

The governing equations are,

$$x_K = A_K(1+\Delta^2) \text{ mod } 2 \qquad (2.20)$$

$$Y_K = B_K(1-\Delta^2) \text{ algebraic} \qquad (2.21)$$

where Δ^2 is 2 bit delay $(e^{-j4\pi fT})$.

The system is explained in Table 2.3.

Table 2.3

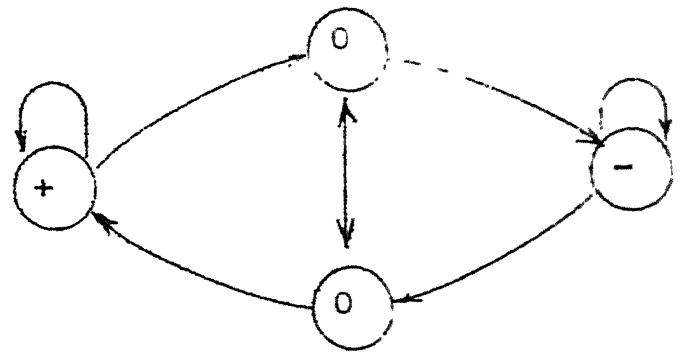
x_K	0	1	0	0	1	1	0	0	0	1	0	1	1	1
A_K	0	1	0	1	1	0	1	0	1	1	1	0	0	1
$B_K = 2a_K - 1$	-1	1	-1	1	1	-1	1	-1	1	1	1	-1	-1	1
y_K			0	0	+2	-2	0	0	0	2	0	-2	-2	2
$x_K (y_K \bmod 2)$			0	0	1	1	0	0	0	1	0	1	1	1

The other method of implementing MDB shown in Fig. 2.8 can be put in similar tabular form.

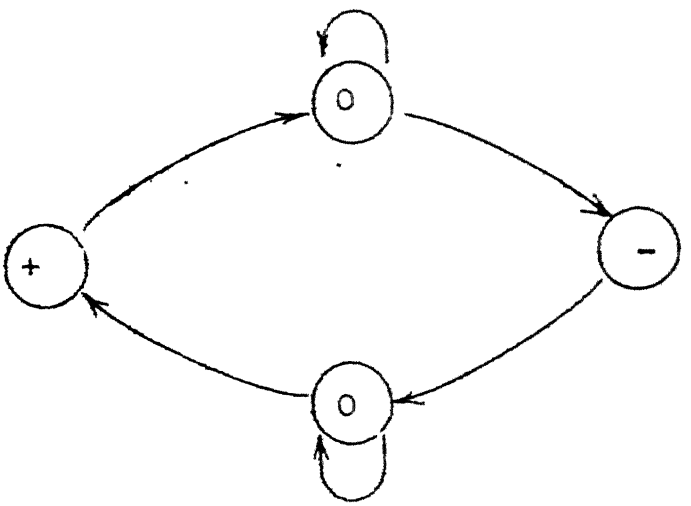
2.2.3 Error Detection in PRS:

In addition to other qualities of the partial response schemes viz. ability to operate at higher rates, spectral shaping etc. these have certain error detection capabilities without the addition of any redundent bits. These can be described with signal state diagrams of Fig. 2.11.

Fig. 2.11(a) shows the signal state diagram for Duobinary. When the number of mid levels is odd between



a) Duobinary



(b) Modified duobinary (even or odd bit stream)

Fig. 2.11: Signal state diagrams (error detection)

two extreme levels, the extreme levels are of different polarities, whereas when the number of zeros (midlevels) is even, the extreme levels have same polarity.

Fig. 2.11(b) shows the signal state diagram for M.DB, only for odd or even bit streams. Both the streams follow

same rule. The extreme levels can not remain same for more than one bit and irrespective of number of zeros in between, the two successive extreme levels have to have differing polarities.

These rules can be monitered and any variation can be used to detect the error condition of the channel. In Fig. 2.12 a general scheme for error detection is given [7].

These signal state diagrams are different from the conventional signal state diagrams in the sense that the zeros (mid levels) shown, constitute the memory of these systems. That is depending upon which zero is reached, the next level is decided. Thus we see that the limited memory which is the key to correlative coding also helps in error detection.

2.2.4 Performance of PRS Systems:

We end this section by discussing the points which can be used to compare the performance of PRS schemes. These are given below.

a) Data rates: As seen in Chapter 1, the PRS schemes can operate at higher data rates compared to simple binary(2n). The duobinary can achieve upto 43% more than Nyquist rate and MDB can go upto 16% more than the Nyquist rate as given by Kabal and Pasupathy [3].

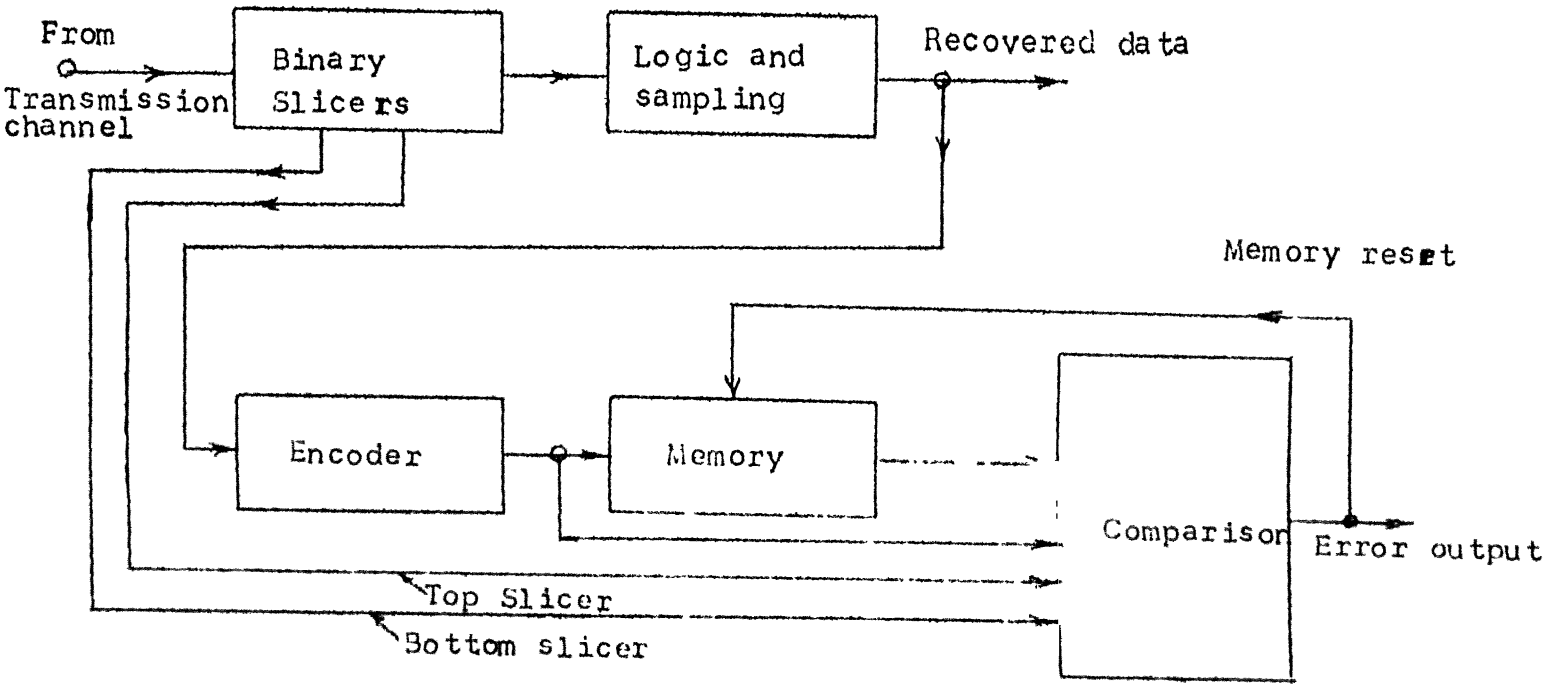


Figure 2.12: General diagram of error detection in PRS.

b) Speed tolerance: The tolerance of zero memory systems, when used at Nyquist rate in Nyquist bandwidth, is zero as seen in Section 1.2.3. The measure of speed tolerance could be the horizontal eye opening available in the eye diagram shown in Fig. 2.13 and PRS systems can operate with some timing jitter.

c) SNR: Due to increased number of levels the PRS systems have SNR degradation of about 3 dB compared to binary systems [7]. The vertical eye opening (Fig. 2.13) is the measure for this. This in turn can tell us about the probability of error.

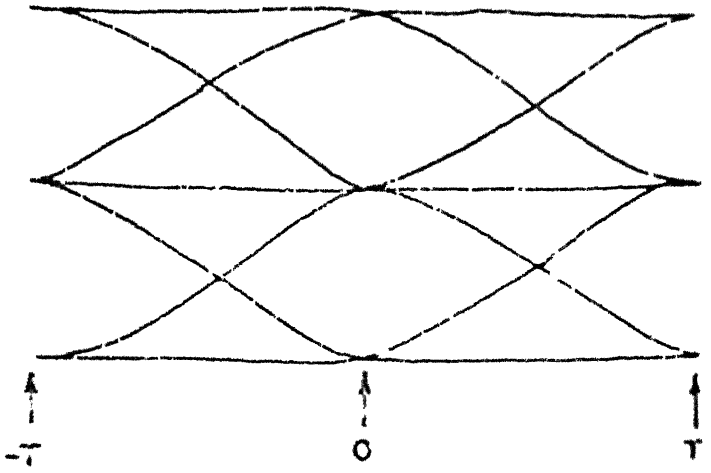
d) Spectral shaping: PRS schemes offer good spectral shaping and can be used in bandlimited channels.

These points will be considered while discussing the performance of the nonlinear implementation of the MDB in Chapter 5.

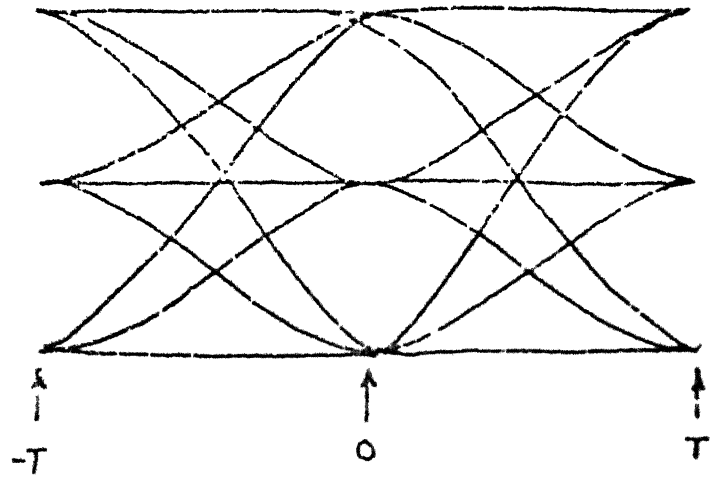
2.3 IMPLEMENTATION OF PRS SCHEMES:

2.3.1 Conventional Implementation:

In the previous section we discussed the Duobinary and MDB schemes. The filter requirement for Duobinary is a quarter cosine filter given in (2.12) and shown in Fig. 2.3. The MDB can be implemented by a low pass filter given by (2.18) and shown in Fig. 2.7.



(a)



(b)

Figure. 2-13: Eye Diagram
(a) Duobinary (b) MDB

The conventional implementation of these filters is critical. The filter has to be designed to fit the curves and match the impedances. Even if MDB is implemented as a combination of delay and an analog duobinary filter as shown in Fig. 2.8, it still needs the duobinary quarter cosine filter.

Lender [7] has given the requirement of the filter for duobinary as well as modified duobinary. The attenuation beyond the cut off frequency, $\frac{1}{2T}$ Hz, is required to be minimum 35 dB. This makes the filters difficult to implement and only approximations are possible. Another drawback is that since the filter has to be designed for a particular frequency, any major change in the data rate changes the filter design and implementation.

2.3.2 Feher's Filter:

Considering the problem involved in designing the filters for correlative coding, Feher [4] suggested nonlinear switching for pulse overlapping to generate ISI and jitter free signalling.

Fig. 2.14 gives a block diagram of the method used by Feher [7].

The principle used by Feher is like this. The two sine waves of opposite polarities and two dc levels are

available and can be sent out on the channel. The signal to be transmitted is decided by the logic based on the data stream and the PRS polynomial used. That is the +ve going sine is sent out say for a logical one. If this bit supplements the next bit (1+D) then +ve DC level will be sent out. If the current bit is to be suppressed due to previous bit then the +ve going or -ve going sine wave is sent depending upon which state was sent earlier so that the output is back to zero(dc)level. The scheme is discussed in [4].

Feher used analog switches (IC 4066) to switch ON/OFF the signals based on the logic. However this could not be extended to higher data rates due to limitations of analog switches. Also the dc levels are critical to avoid glitches which in any case occur at the switch-change instances.

2.3.3 Translinear Implementation of PRS:

In this thesis the concept of nonlinear waveshaping is used for correlative coding. The nonlinear switching is done entirely by Gilbert cells. The control signals are of low amplitudes and cause no jitter in the output. The method is modular and can be used for any PRS polynomial. The block diagram of the nonlinear waveshaping implementation used for MDB, is shown in Fig. 2.15.

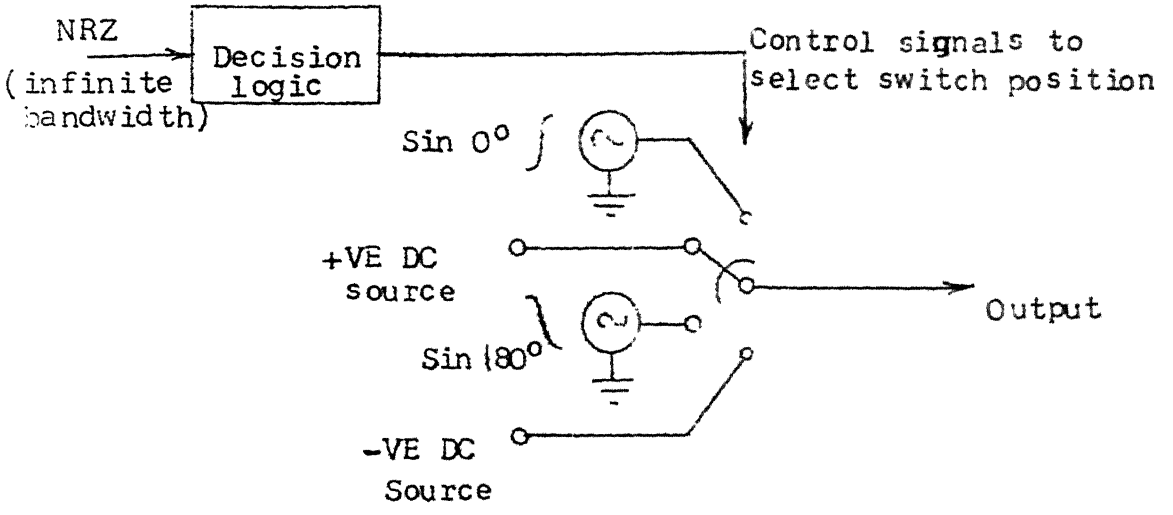


Figure 2.14: Feher's Nonlinear Filter

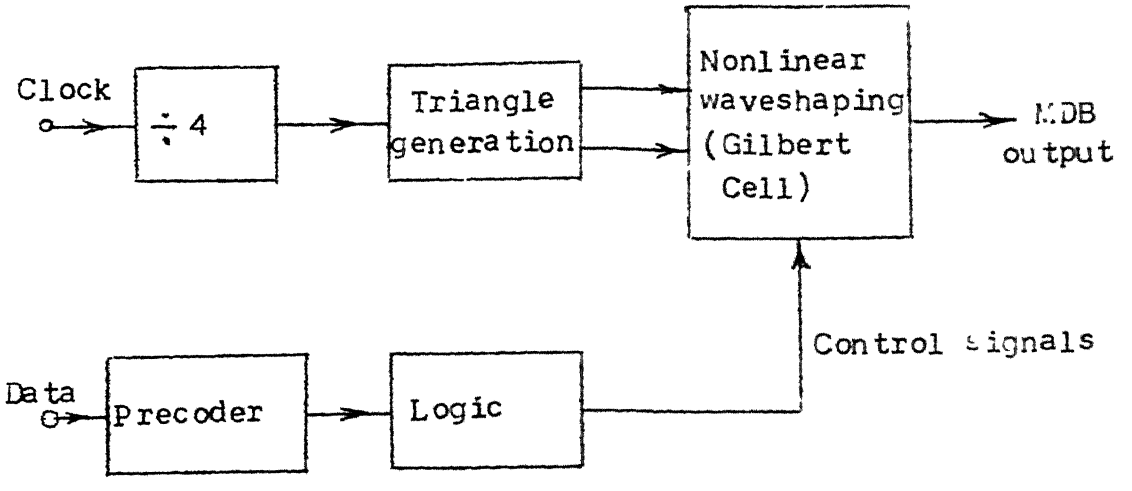


Figure 2.15: Translinear implementation of PRS

The scheme gives good eye opening and bit error rates. The out of band power is minimum and a simple LPF at the output can bandlimit the signal. The detailed implementation is discussed in the next chapter.

CHAPTER 3

REALIZATION OF PRS BY TRANSLINEAR CIRCUIT

The conventional realization of the PRS by analog filters was discussed in Chapter 2. Feher's nonlinear wave-shaping method was discussed. In this chapter the nonlinear wave-shaping technique is extended to operate at much higher data rates. Gilbert cells or bipolar transistor version of the double balanced four quadrant modulator/demodulator is used for switching to achieve this.

The Gilbert cell is described, followed by its use for our purpose. The actual implementation of MDB is subsequently given. It is shown that this method can be extended to any other PRS polynomial.

3.1 THE BASIC BUILDING BLOCK:

The basic building block used for realizing the PRS polynomials is described below.

3.1.1 The Emitter Coupled Pair:

A typical circuit with emitter coupled transistor pair is shown in Fig. 3.1.

The collector currents IC1 and IC2 are given by equations (3.1) and (3.2) [9].

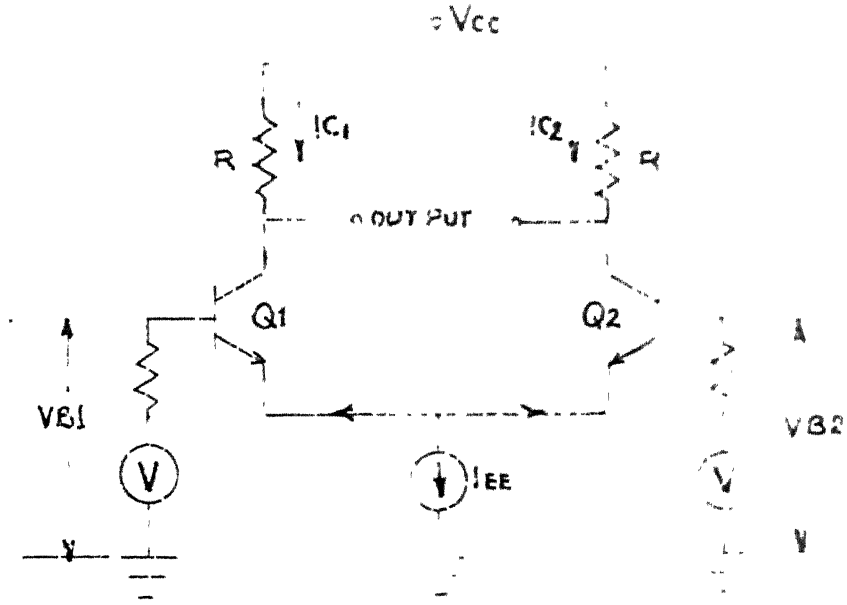


Figure. 3·1 : Emitter Coupled pair.

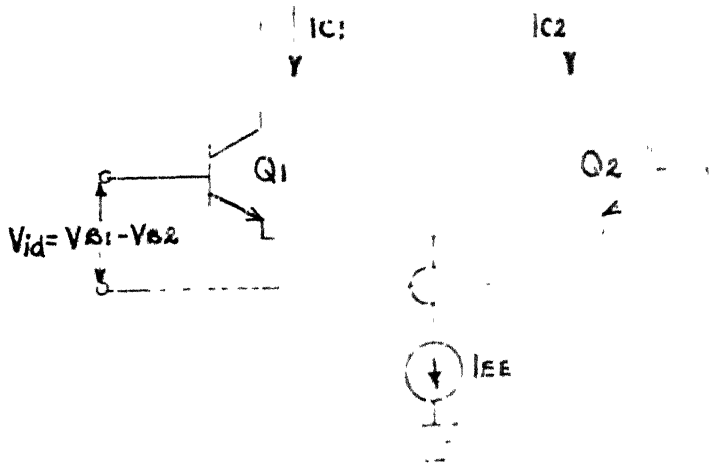


Figure. 3·2 : Emitter Coupled pair

$$IC1 = \frac{IEE}{1 + \exp[-\frac{Vid}{VT}]} \qquad (3.1)$$

$$IC2 = \frac{IEE}{1 + \exp[\frac{Vid}{VT}]} \qquad (3.2)$$

where $Vid = (VB1 - VB2)$ (3.3)

and VT is the volt equivalent temperature which is 26 mV at room temperature. Fig. 3.2 shows the same emitter coupled pair with only relavent details.

From (3.1) and (3.2) the difference between the collector currents can be written as

$$\Delta IC = IC1 - IC2$$

$$= IEE \cdot \tanh(\frac{Vid}{2VT}) \qquad (3.4)$$

This difference of collector currents gives the transfer characteristics of the circuit and is plotted in Fig. 3.3.

The transfer characteristic is linear in a small region in centre where Vid is smaller than VT and nonlinear otherwise. Assuming Vid to be small (3.4) can be written as

$$\Delta IC = IEE(\frac{Vid}{2Vt}) \qquad (3.5)$$

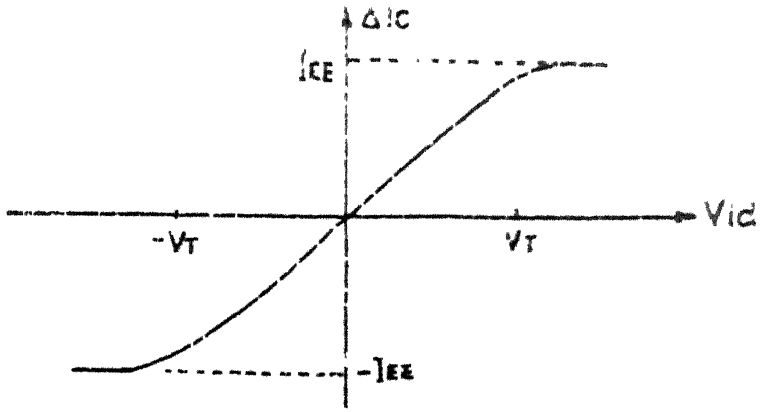


Figure 3.3 : Tranfer characteristics of Emitter coupled pair

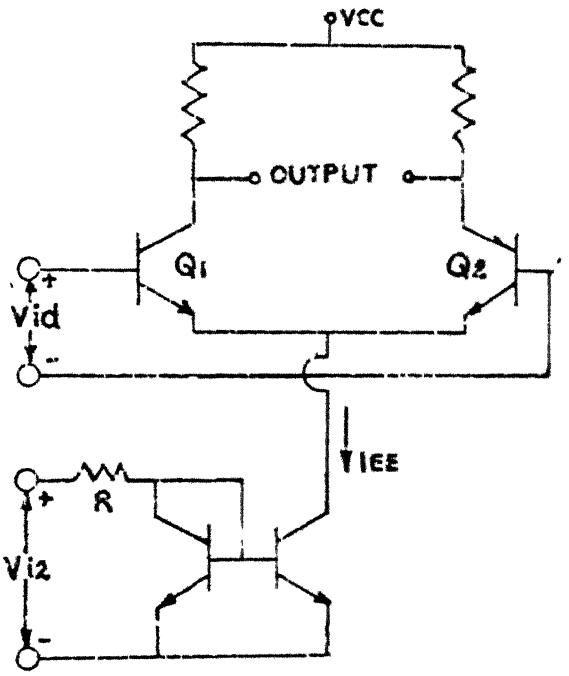


Figure.3.4 : Analog multiplier

3.1.2 Emitter Coupled Pair as Multiplier:

If the current IEE in (3.5) is made dependent upon other voltage say v_{i2}. then the output will be in effect a product of v_{i2} and Vid. This is shown in Fig. 3.4.
So we write

$$IEE = K \cdot (Vi2 - VBE(ON)) \qquad (3.6)$$

From (3.5) and (3.6)

$$\Delta IC = \frac{K(Vi2 - VBE(ON)) \times Vid}{2VT} \qquad (3.7)$$

Thus we have a voltage multiplier under following assumptions:

a) Vid is small compared to VT

b) V_{i2} is large compared to VBE(ON)

3.1.3 The Gilbert Cell:

The Gilbert cell is a modification of the multiplier circuit explained in Section 3.1.2. Two of these multipliers are cross tied as shown in Fig. 3.5.

The various collector currents IC1 to IC6 can be written using (3.1) and (3.2) and using these the difference current ΔI can be written as under [9].

$$\Delta I = IA - IB$$

$$= IEE \times \tanh\left(\frac{V1}{2VT}\right) \times \tanh\left(\frac{V2}{2VT}\right) \qquad (3.8)$$

Thus we see that the output, proportional to ΔI is product of tan hyperbolic of two inputs V_1 and V_2 provided both are small compared to VT.

If one input is large compared to VT, the transistor pair to which this voltage is applied acts as a switch, thereby effectively multiplying the other small signal by a square wave. It is this circuit that is being used for our 'Basic Building Block'.

3.1.4 Gilbert Cell as Basic Building Block:

Consider the Gilbert cell of Fig. 3.5. If a large voltage (V_2) is applied to one of the two transistors Q_1 or Q_2 the current drawn by that branch increases thus decreasing current in the other branch. Thus the small signal (V_1) given to the cross coupled pair appears at the output as if it is multiplied by one or zero or -1 or zero depending upon which branch is carrying more current.

The larger voltage V_2 is given logical high/low (5V/2.5V). The effect of these voltages on the output is given in Table 3.1.

Thus the base signals at Q_1 and Q_2 are used to allow or block the small signal (V_1) to appear at output , in or out of phase with input signal. This basic building block is used for realizing the PRS schemes.

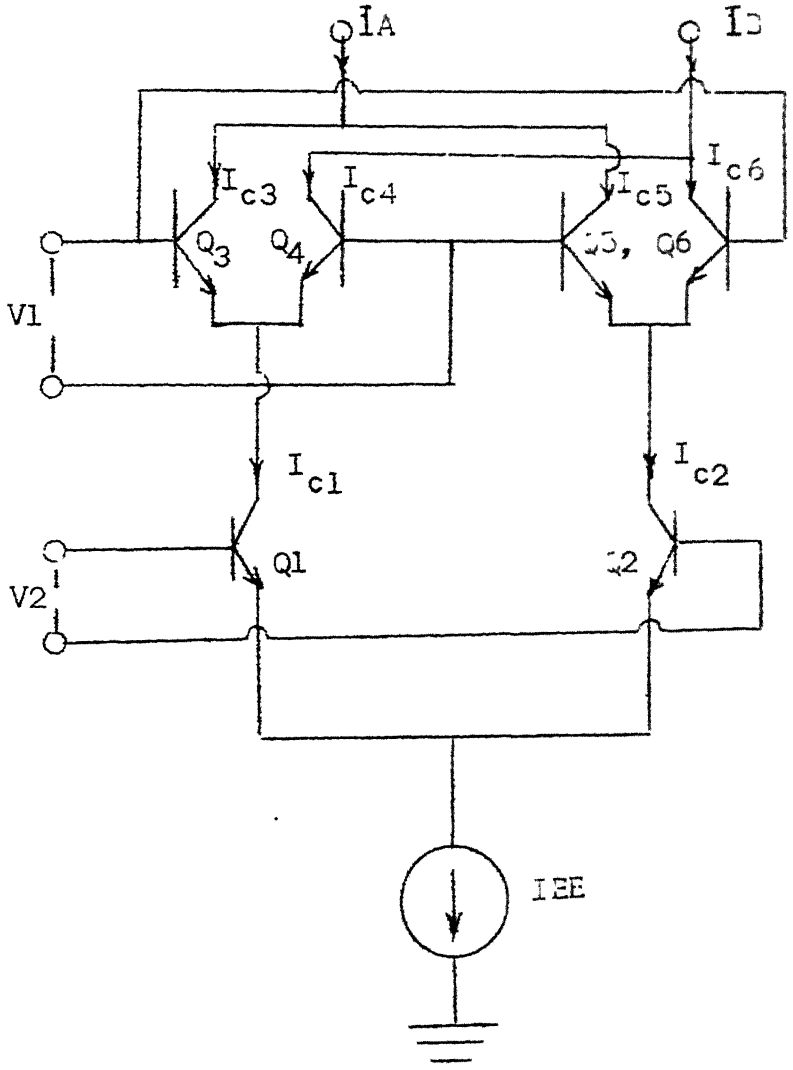


Figure 3.5: Gilbert Cell

Table 3.1

	Q_1	Q_2	Output
Case 1	H	H	0
Case 2	L	L	0
Case 3	H	L	Follows input
Case 4	L	H	Follows inverted input

H : High (3V)

L : Low (2.5V)

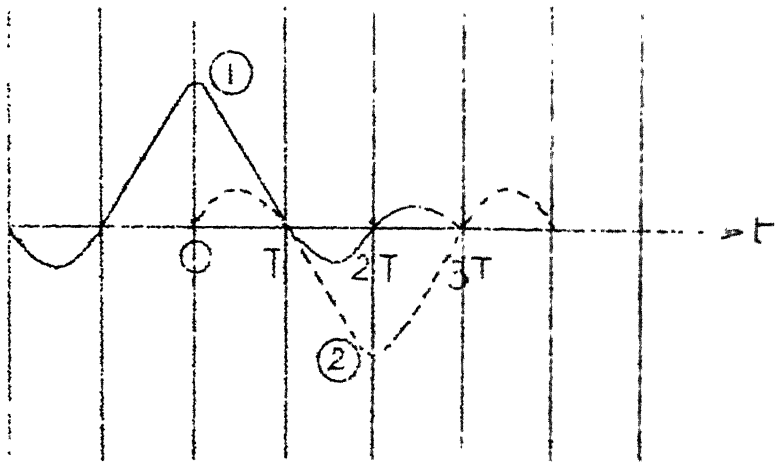
3.2 IMPLEMENTATION OF PRS SCHEME USING BASIC BUILDING BLOCK:

In this section the realization of MDB using the basic building block is explained.

3.2.1 Modified Duobinary (MDB):

As seen in Section 2.2.2 the MDB introduces interference after one bit delay and in phase opposition ($e^{j\pi}(1-D^2)$). The MDB is characterized by (3.9) and its impulse response is shown in Fig. 3.6.

$$h(t) = \frac{\sin\pi t/T}{\pi t/T} - \frac{\sin\pi(t-2T)/T}{\pi(t-2T)/T} \qquad (3.9)$$



(1) Impulse response $\frac{\sin x}{x}$

(2) Phase reversed and delayed ISI due to (1)

Fig. 3.6: Impulse response (MDB)

From Fig. 3.6 it appears that the ISI in current bit is due to the bit prior to the past bit. If the data stream is split into two streams of odd and even bits the output for each of these odd and even bits is affected as shown in Table 3.2.

Table 3.2

Case	Past bit	Present bit	Output
1	0	0	No output
2	1	1	No output
3	0	1	$\frac{\sin x}{x}$ output for two bit durations
4	1	0	Same as case 3 but phase reversed

This required output is obtained by the basic building block. Two of such blocks are used for odd and even streams and their outputs combined to get MDB signal.

3.2.2 MDB using Basic Building Block:

The data stream is split into even and odd streams. Each is processed by a Gilbert cell. The clock is divided down and integrated to obtain triangle waveforms of four clock durations. This clock when ac coupled to the small signal input has triangle waveforms of two bit durations as required. These triangles are either +ve going or -ve going.

Using the data stream (odd/even) of two clock durations the triangle is allowed to pass to the output of the Gilbert cell. The triangle depending upon its amplitude follows the 'tanh' characteristic of the Gilbert cell as given in Fig. 3.3 and appears at the output in required smoothened form.

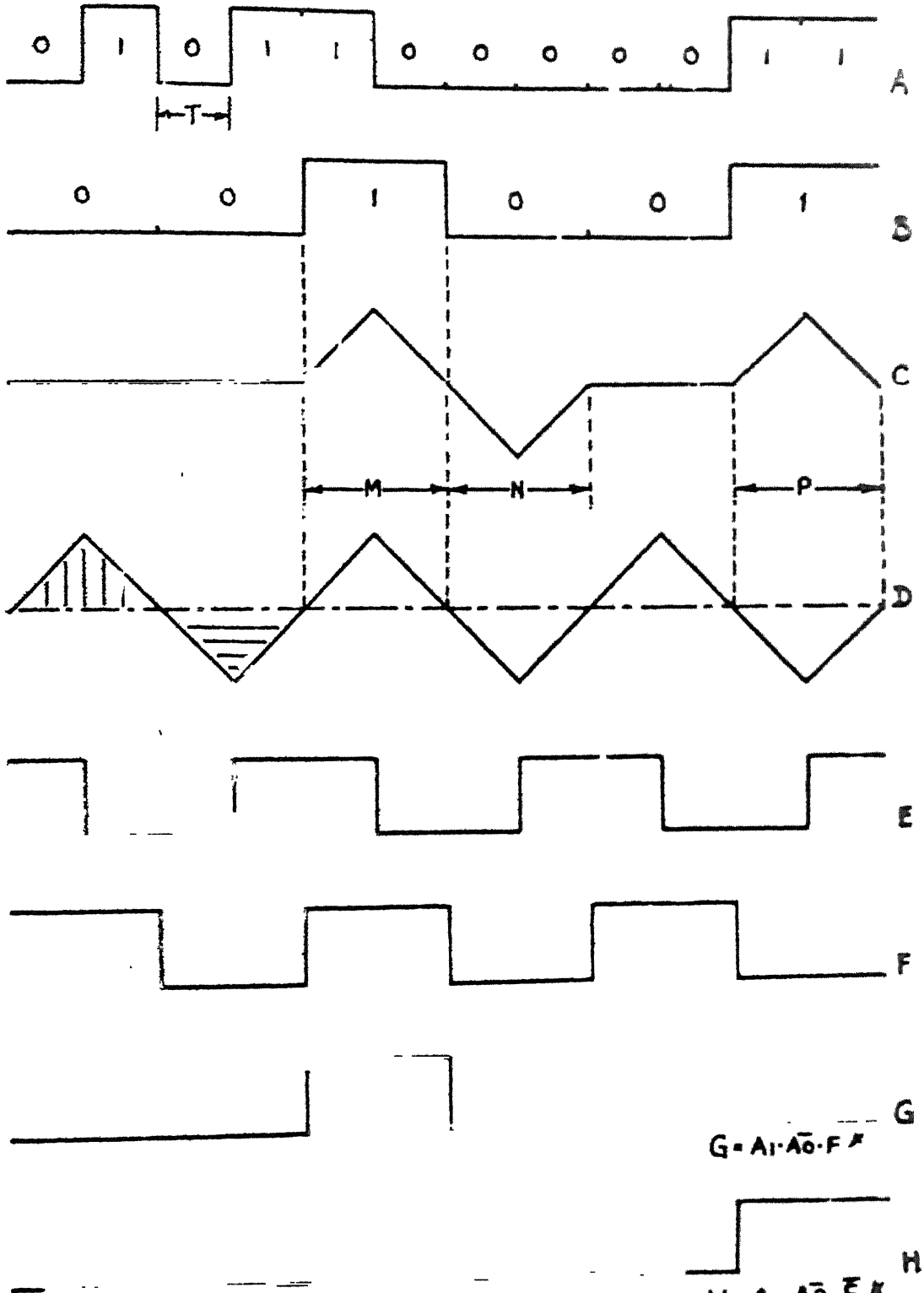
The triangle is allowed to pass to the output only for 1-0 or 0-1 combinations of the data stream. Also since we want, say +ve triangle for 1-0 and a -ve triangle for 0-1 combination and only one type of triangle is available in the time slot (2 CK durations), another clock is monitored to indicate if a +ve or a -ve triangle will be available in that time slot and based on this and the 1-0 or 0-1 combination of data

control signal is given to one of the two switching transistors (Q_1/Q_2 of Fig. 3.5) so that a correct triangle either +ve or -ve is available at output.

Exactly similar processing is performed with the other data stream and finally these two outputs are added. This is achieved by tying the collectors of two Basic Building blocks to get the final MDB output. The various waveforms are shown in Fig. 3.7.

Fig. 3.7(A) is the precoded data stream and (B) is the odd bit stream. The required output for this is shown in (C). The output exists only for 1-0 or 0-1 combination in data stream (B). The triangle shown in (D) derived by integrating (E) is switched on/off and passed noninverted or inverted to the output.

Consider time slots M and P of Fig. 3.7. In both these a one follows a zero and in both cases a +ve triangle is required at output. However although a +ve triangle exists during slot M, a -ve triangle is available during slot P. So for same combination of zero - one the triangle should be uninverted during M and inverted during P. To achieve this square wave of Fig. 3.7(F) is monitored. Logic based on data (current and previous bit of one data stream) and slot monitor waveform (Fig. 3.7 (G and H)) controls the control inputs of Basic Building Block.


0 1 0 1 1 0 0 0 0 0 1 1
A
T
0 0 1 0 0 1
B
C
M
N
P
D
E
F
G
G = A1·Ā0·F ★
H
H = A1·Ā0·F̄ ★
★ {A0: previous bit
A1: current bit

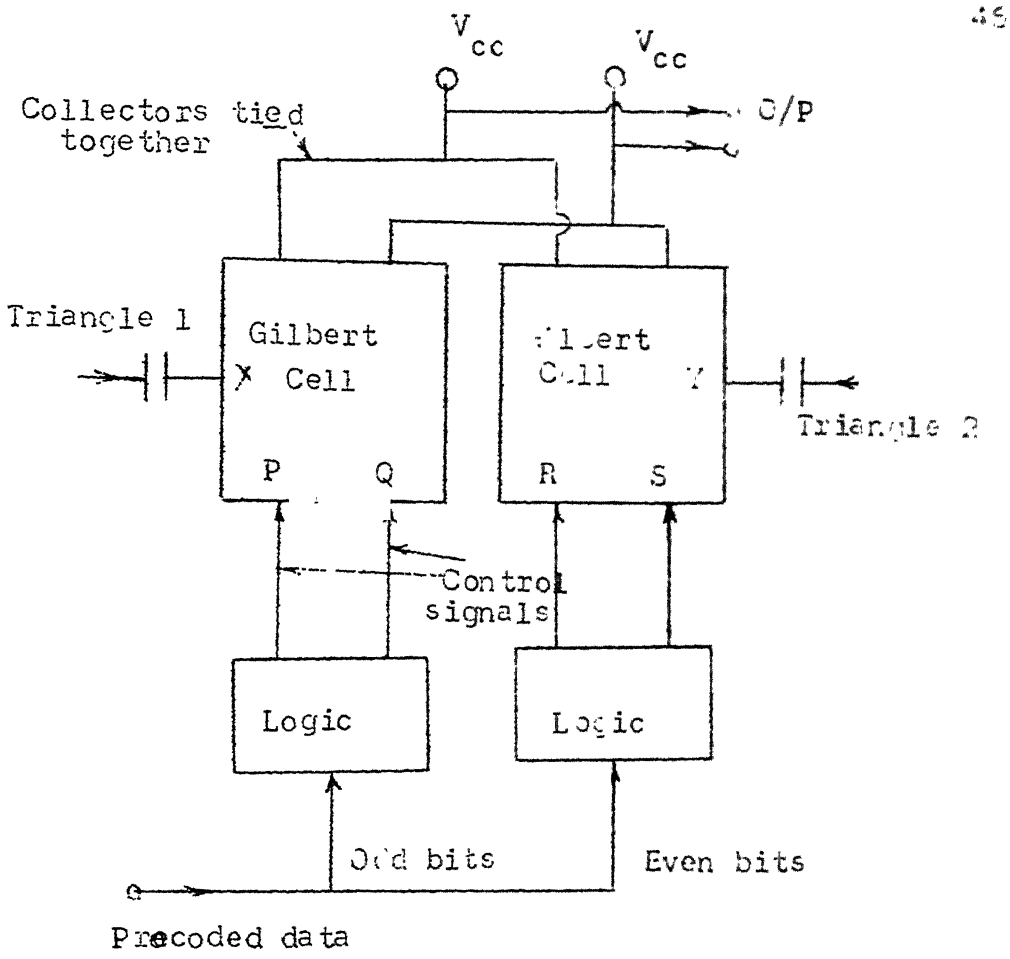
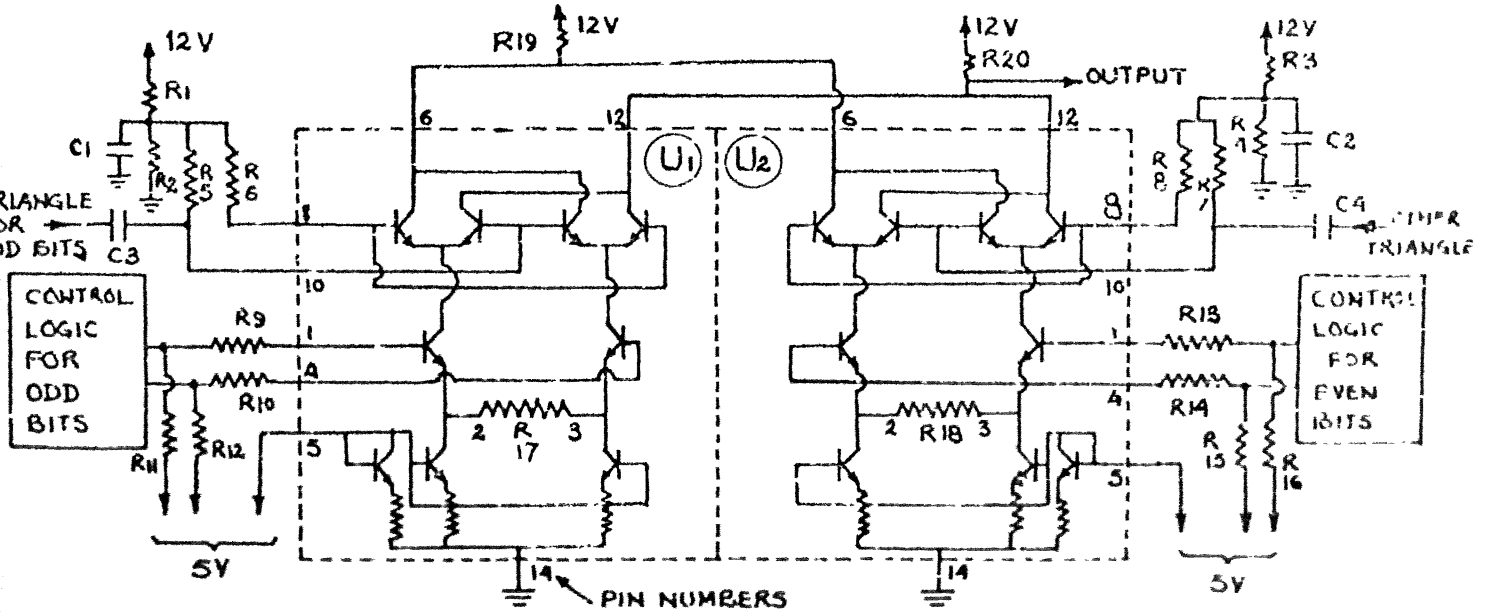


Figure 3.8: Block diagram - MDB realisation



R1 - R4	- 3.9 KOHM
R5 - R8	- 100 OHM
R9 - R16	- 1.5 KOHM
R17 - R18	- 680 OHM
C1 - C4	- 0.1 μF
U1 - U2	- IC 7486

Figure.3.9 : Schematic diagram - MDB realization.

Other (even) bit stream (C) is processed similarly by other basic building block. Now waveform of (E) is used for slot monitoring and (F) is used to get required triangle.

Fig. 3.8 shows the block diagram of MDB realisation. The schematic diagram of this is shown in Fig. 3.9 less the driving logic generation circuitary. The schematic diagram of IC 796 used is attached at Appendix 'C'.

3.2.3 Design of Control Logic:

Ref. Fig. 3.8. The two triangles of four clock durations each at 90^{o} phase difference, obtained by integrating wave forms of Fig. 3.7(E) and (F) are applied to the small signal inputs X and Y of the two Gilbert cells. The two cells are coupled together by connecting their collectors. Each cell processes either the even or odd data stream.

When the triangle of Fig. 3.7(d) is given to point X of Fig. 3.8 the relevant controls P and Q should be such that Table 3.3 is satisfied.

Similar pattern must be followed by other control inputs R and S based on the other data stream. The complete timing diagram including MDB output is shown in Fig. 3.10 and the control steering logic for control signals P, Q, R and S is generated as shown in Fig. 3.11.

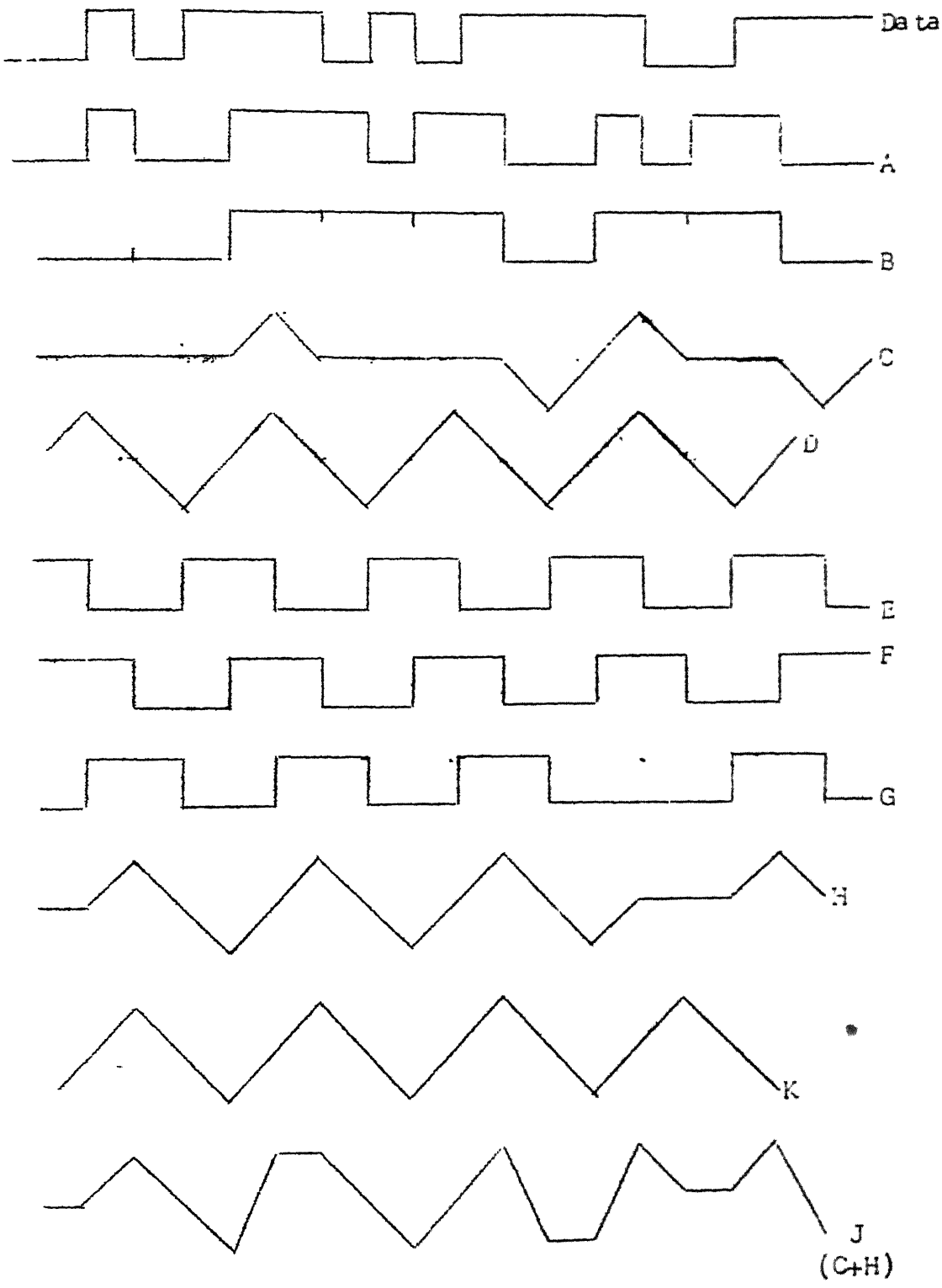
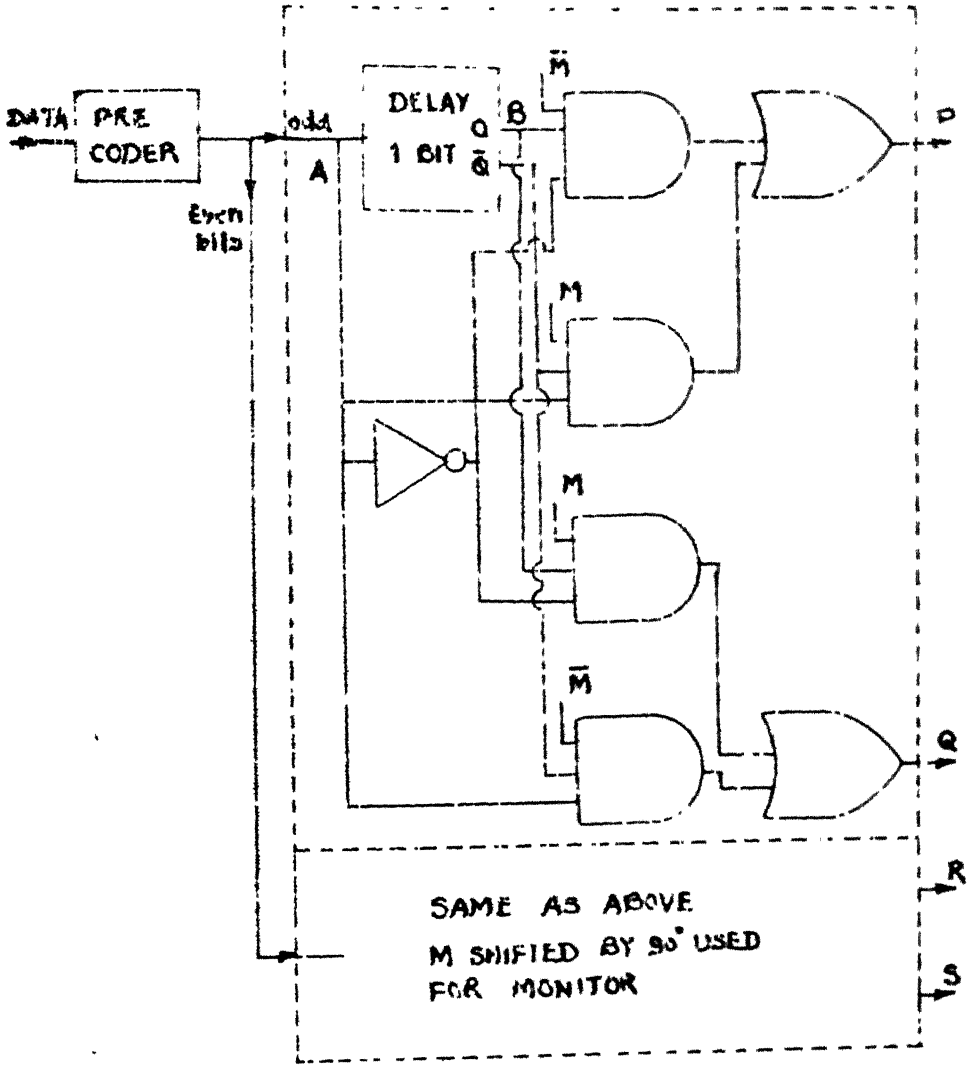


Fig. 3.10. Timing diagram – MDB



M : Moniter waveform to decide inversion or otherwise.

Logic : $P = A\bar{B}M + \bar{A}B\bar{M}$

$Q = A\bar{B}\bar{M} + \bar{A}BM$

where A - current bit
B - past bit

Steering control logic

Table 3.3

Past bit	Present bit	Type of triangle available* (Fig. 3.7(f))	P	Q
0	1	1	H	L
0	1	0	L	H
1	0	1	L	H
1	0	0	H	L
1	1	X	L	L
0	0	X	L	L

* 1 : +ve triangle
0 : -ve triangle
H : High
L : Low
X : High or low

3.3 HARDWARE IMPLEMENTATION, MDB:

The previous section described how the MDB can be realized using the basic building blocks and the control signals. The actual hardware implementation is discussed in this section alongwith the finer points considered for actual implementation. Fig. 3.12 gives the block diagram of the duobinary transmitter and various block are

subsequently discussed. The actual implementation is done at 500 KHz clock frequency. The complete schematic diagram of transmitter is attached at Appendix B.

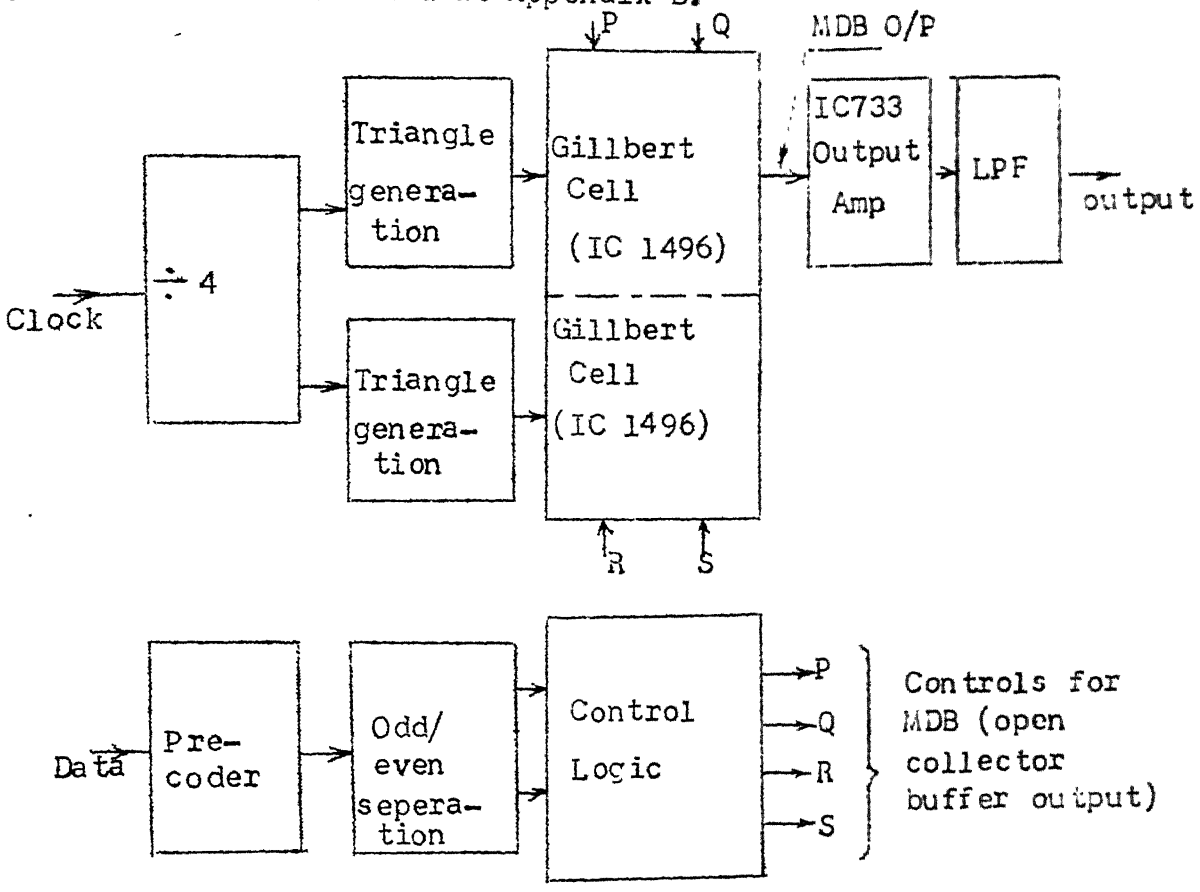
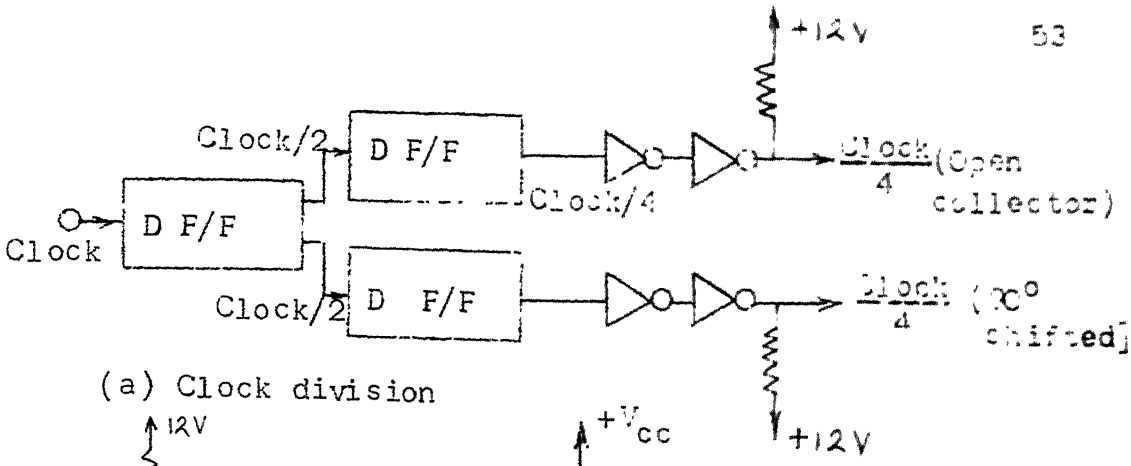


Fig. 3.12: Block diagram, MDB transmitter.

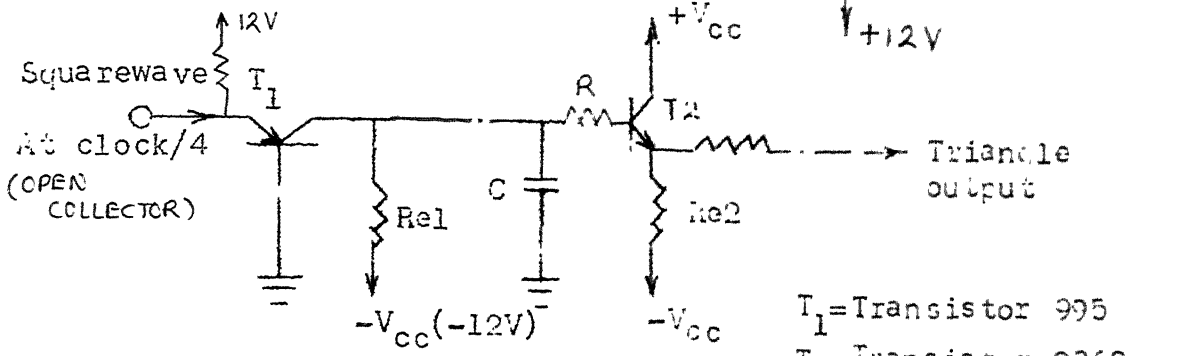
The various smaller circuits explained below are shown in Fig. 3.13.

3.3.1 Triangle Generation:

The clock is divided by 4 in two steps using D flip flops as shown in Fig. 3.13(a). These two clocks (clock/4)



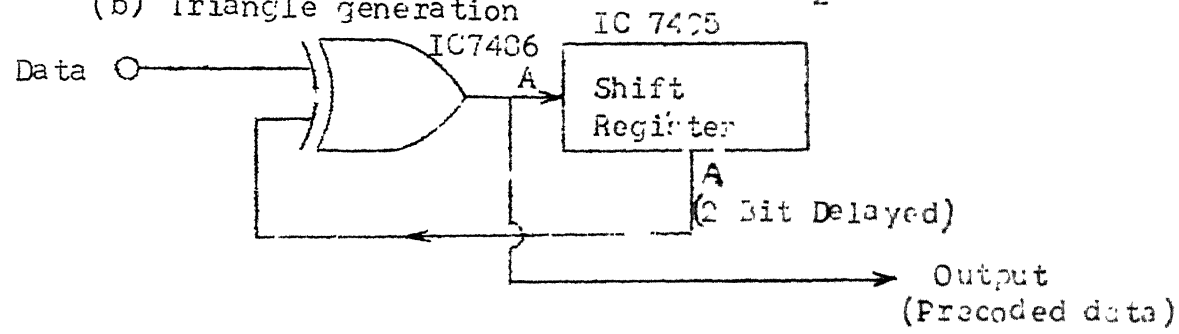
(a) Clock division



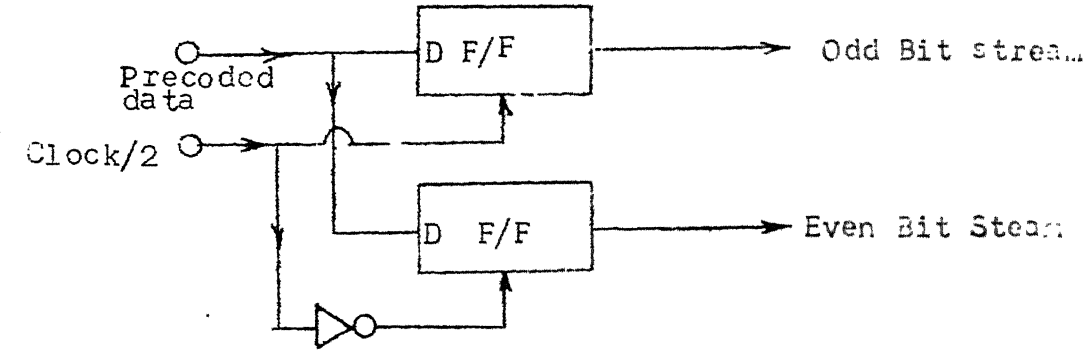
T_1=Transistor 995

T_2=Transistor 2369

(b) Triangle generation



(c) Precoder for nDB



(d) Seperation of even and odd bits

are integrated to get the triangles. The circuit is shown in Fig. 3.13(b). It is a simple RC circuit. Re_1 provides discharge path for C. It is followed by an emitter follower T2. These triangles are ac coupled to the small signal inputs of the two Gilbert cells.

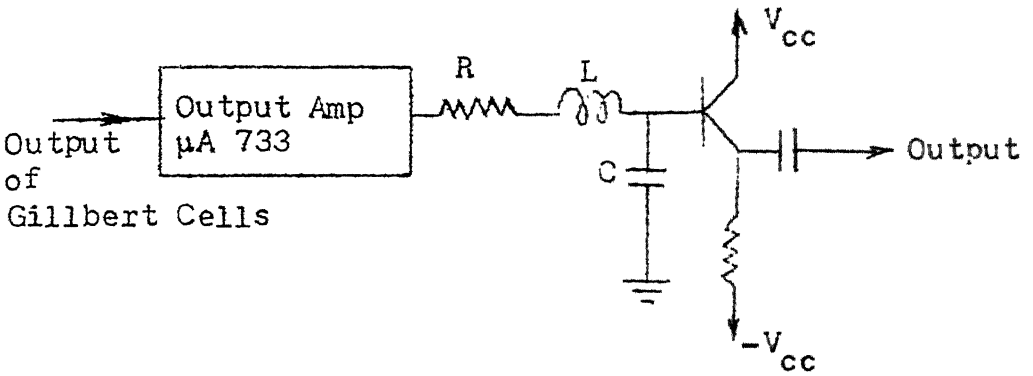
3.3.2 Steering Logic Generation:

The data is precoded by the circuit of Fig. 3.13(c) to avoid error propogation as discussed in Chapter 2. The seperation of precoded data into odd and even bit streams is done by circuit of Fig. 3.13(d). The final control signals which depend on these odd and even streams are generated as already explained (Fig. 3.11). The control signals are buffered with open collector buffers using a matched resistor network such that 5V is extended when the logic is high but 2.5V is extended to Gilbert cell when logic is low.

3.3.3 The Output Stage:

The output of the two Gilbert cells added together takes two levels on +ve and -ve sides. That is, the output level is different if only one (odd/even) stream allows a triangle but changes level when two overlapping triangles on same side are added. This problem is taken care of by the output amplifier. A differential video amplifier μA 733 is

Finally a simple second order L-C low pass filter with cut-off frequency of about 200 KHz is used at the output to bandlimit the signal without distortion. This is followed by an emitter follower used as line driver. The output stage is shown in Fig. 3.14.



R = 470

L = 330 mH

C = 1500 pf

Fig. 3.14: Output stage MDB transmitter.

3.3.4 Some Finer Points:

Some finer points in the implementation are given below.

i) The introduction of emitter degeneration resistors in the Gilbert cells will make the transfer characteristic more linear and higher data rates can be possible.

ii) Since control signals are given by logic, these may be slightly delayed as compared to the triangles. As

such, a small variable delay, in the clock used for triangle generation, may be used to avoid glitches in the output.

iii) The two Gilbert cells outputs can be individually checked to ensure that each of it is without a dc component. (Reference Fig. 3.7(c)).

iv) Although the circuit is designed for clock frequency of 500 KHz, it can easily be operated at much higher data rates by minor changes. The values of R and C of integrator of Fig. 3.13(b) have to be changed for perfect triangle output and the LPF at the output may have to be changed. Rest of the circuit requires no change.

3.4 SPECTRAL SHAPING DUE TO WAVESHAPING:

Since the transfer characteristics of the Gilbert cells are translinear (linear at the centre and nonlinear otherwise) as shown in Fig. 3.3, the triangle truncation and amplitude plays an important role in the output. When the signal input is small the output follows it but when it is more, the output is smoothened out.

An exercise was carried out to find the ideal height of trapezoidal output, (we consider the complete MDB generator to have various transfer characteristics(in time), triangle and then triangle with its top cut-off forming a trapezoid, the limit being a rectangle) which gives minimum out of band

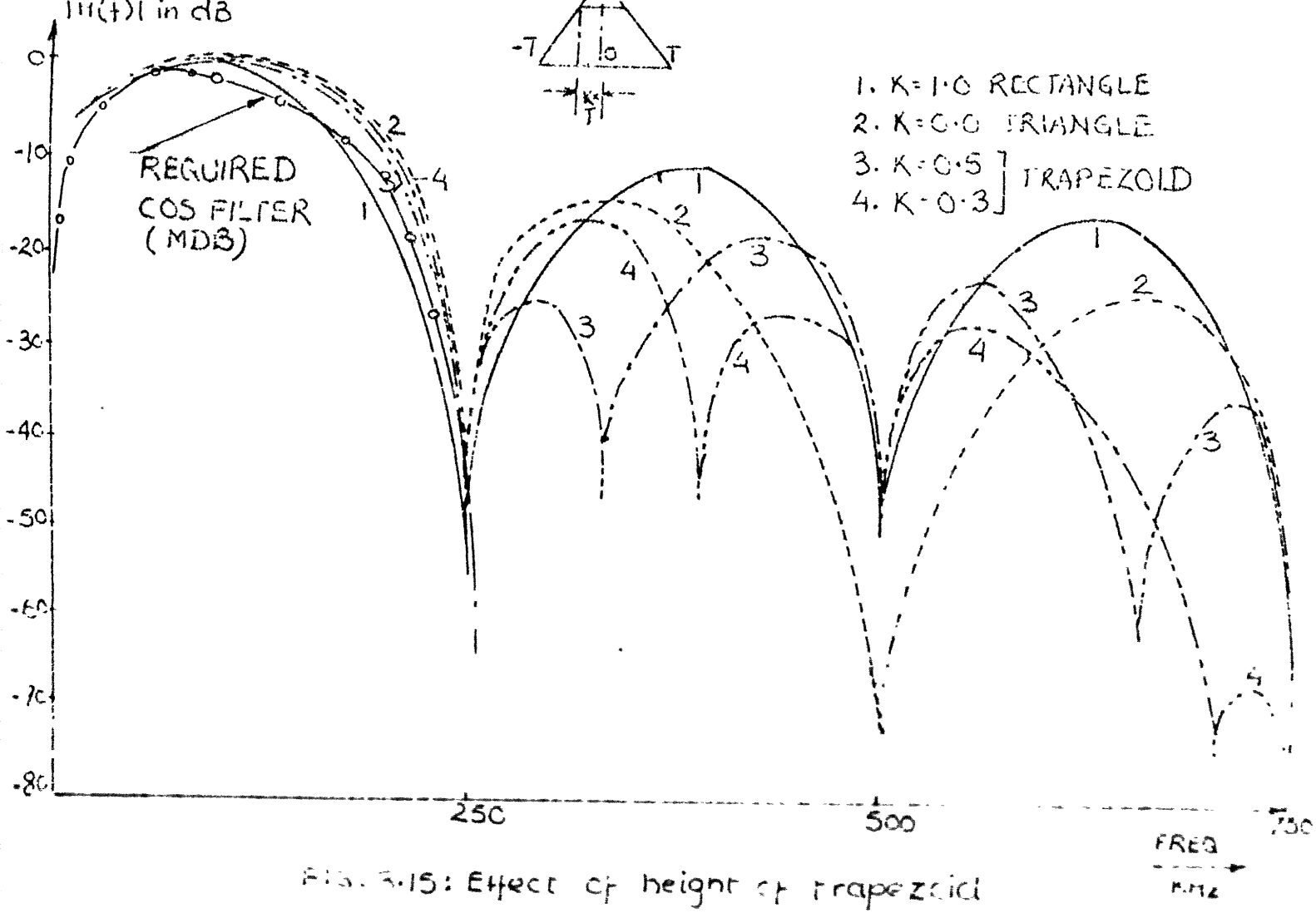


FIG. 3.15: Effect of height of trapezoid on spectral shaping.

spectral power. All the trapezoids were normalized for equal energy content. It emerged that triangle cut at 0.4 times its normal amplitude as output gives best results. The details are attached at Appendix D and Fig. 3.15 shows the obtained results.

3.5 EXTENSION OF THE TECHNIQUE TO OTHER PRS POLYNOMIALS:

As seen in previous chapter, various PRS polynomials are possible. The advantage of the scheme presented for MDB is that it can be very easily extended to any PRS polynomial without any significant changes in the system hardware. In following subsections these implementations are explained.

3.5.1 Duobinary Implementation:

The normal duobinary scheme is characterized by system polynomial (1+D). That is, each bit is going to affect subsequent bit. To implement this we use one Basic Building Block to pass normal or inverted triangle for the current bit and another block for the previous bit. Again the two blocks are coupled together. This is shown in Fig. 3.16.

Now if we want to realize the polynomial (1-D), the only thing we need to do in the circuit of Fig. 3.16 is to interchange the collector inter-connections of two Gilbert cells.

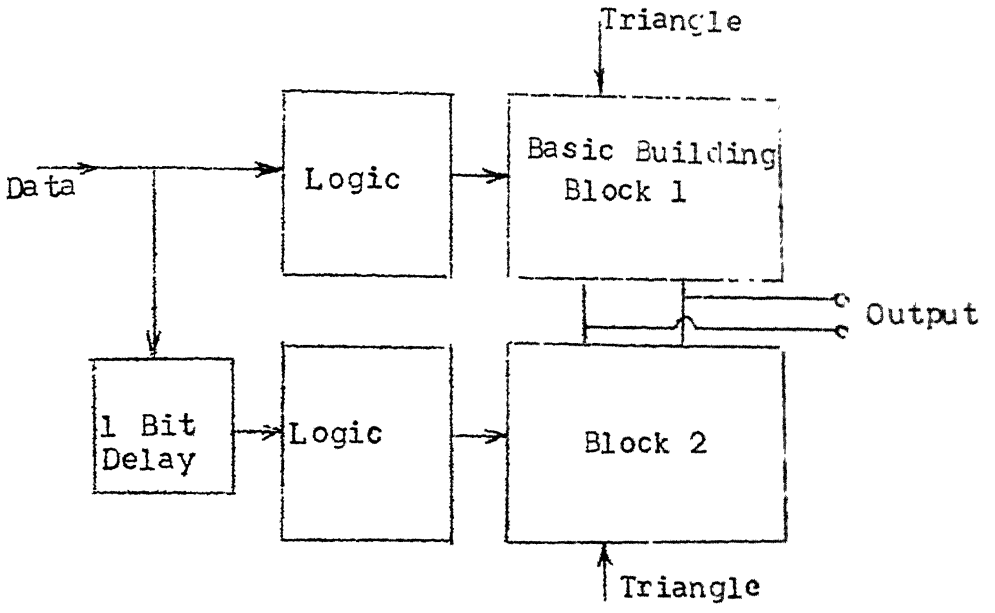


Fig. 3.16: Duobinary realization

Similarly if we have another Basic Building Block, controlled by 2 bit delayed data, we can again realize any polynomial containing 1,D and D^2 with these three blocks. Otherwise we can develope independent logic for the required polynomial and realize it using Basic Building Blocks.

3.6 ADVANTAGES OF WAVESHAPING:

In this chapter it is shown how the MDB filter can be realized using nonlinear waveshaping. It is also shown as to how the technique is moduler in nature and how it can be extended to any PRS polynomial. The circuit can be driven by ECL or TTL logic. It has low voltage levels for switching and exploits the non-saturating current steering and commutation capabilities of the Gilbert-cells. Potentially

the circuit is capable of processing the digital data in Megabits/sec range.

The resulting waveform exhibits clear and broad eye-patterns. By exploiting the tan-typerbolic transfer characteristics of the emitter coupled pair, it minimizes the out of band power and is quite insensitive to variation in transmission data rate.

Some practical advantages are that it is realizable in integrated form. Only two capacitors and two resistors need be changed for various choices of data rates from Kilobits to megabits per sec. The simple second order low pass filter at the output takes care of out of band band power and the scheme can meet CCITT requirements for an MDB digital data link.

CHAPTER 4

PERFORMANCE OF THE SYSTEM

In the previous chapters the PRS scheme implemented by waveshaping was discussed. The system was tested to gauge its performance.

The various tests recommended in the literature [3,6,7,8] are as under.

a) Sensitivity to timing errors: The sensitivity of the system to timing errors can be divided into two parts

i) Speed tolerance

ii) Minimum eye width required

The tolerance is the sensitivity of the system to changes in signalling speeds, assuming the sampler changes phase accordingly. The minimum eye width required, on the other hand is a measure of sensitivity of the system to changes in sampler phase, assuming the transmission speed to be constant.

The decision threshold was kept at the centre of the levels and sampler phase kept at a point where eye opening is maximum. With this if the speed is increased. At certain speed the eye closes. Speed tolerance can also be defined as the increase in transmission rate at which the

smallest eye opening is zero. The speed tolerance for MDB is given as 15.5% [3].

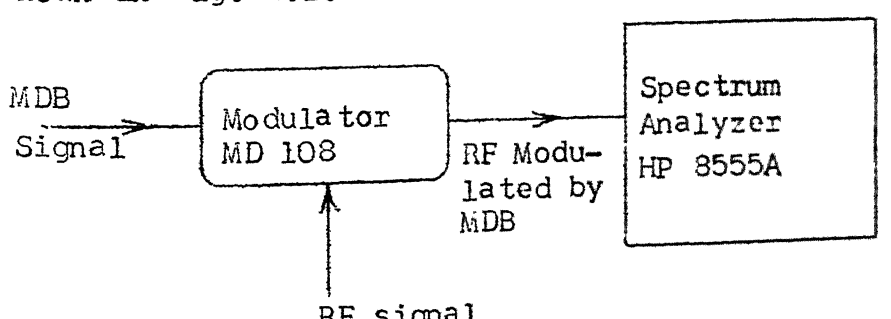
b) SNR degradation: The PAM schemes due to their extra levels have inherent SNR degradation. Whenever the noise is more than the comparator levels it causes error in detection.

c) Spectral shaping: The partial response signalling shapes the frequency spectrum. Minimum out of band power ensures reduced adjacent channel interference. The 'INTELSAT single channel per carrier (SCPC) satellite system' requires that the out of band power at 1.4 times Nyquist frequency should be more than 26 dB down from the inband power [4].

With these requirements the various performance tests were carried out on the system. These are given below.

4.1 SPECTRAL POWER CONTENT:

The MDB waveform after the LPF in the TX stage was observed on spectrum analyzer HP 8555A. The test set up is shown in Fig. 4.1.



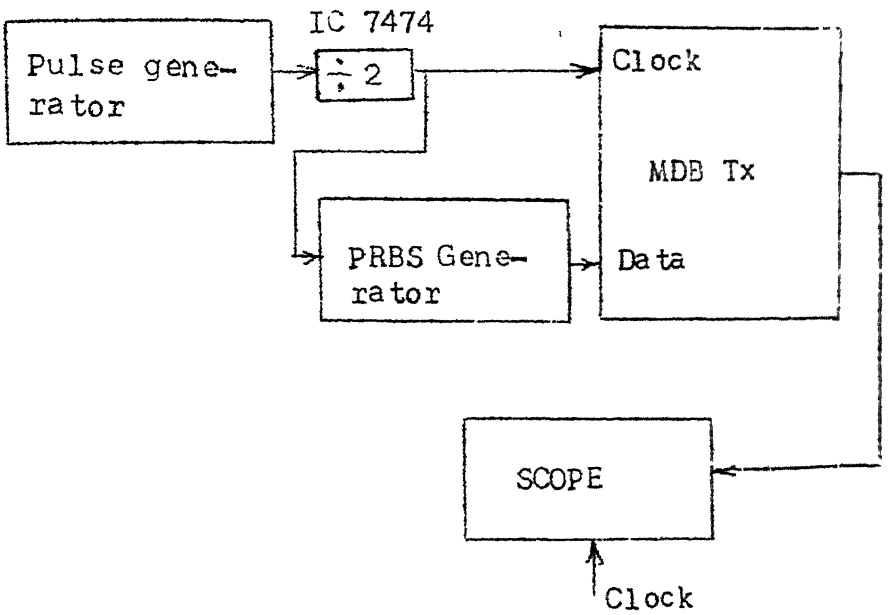


Fig. 4.2: Speed tolerance measurement

is increased the eye starts closing and at one point it closes and can not be adjusted by adjusting clock phase. The frequency of clock at this instance is measured. The speed tolerance is the increase in transmission rate over Nyquist rate at which eye closes. The measured result was about 12-13% for MDB.

4.5 SNR DEGRADATION:

To observe the effect of SNR degradation the measure used was the Bit Error Rate (BER) at various SNR. The test set up is shown in Fig. 4.3.

Error detector HP 3761A is used to monitor the bit error rate of the received data. Noise was introduced using

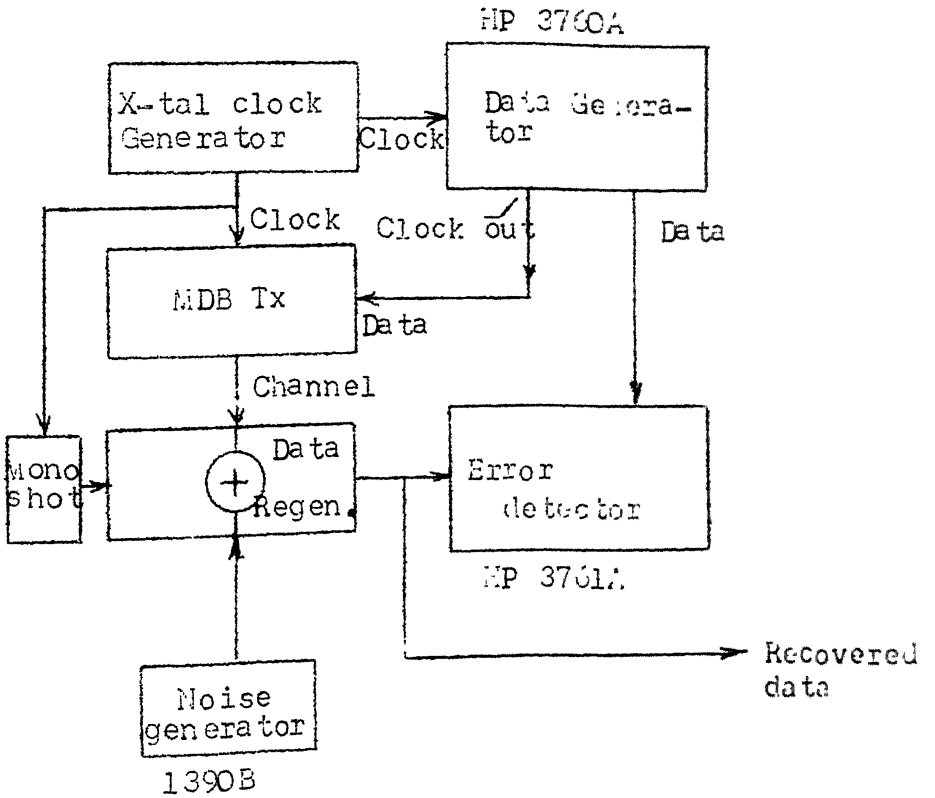


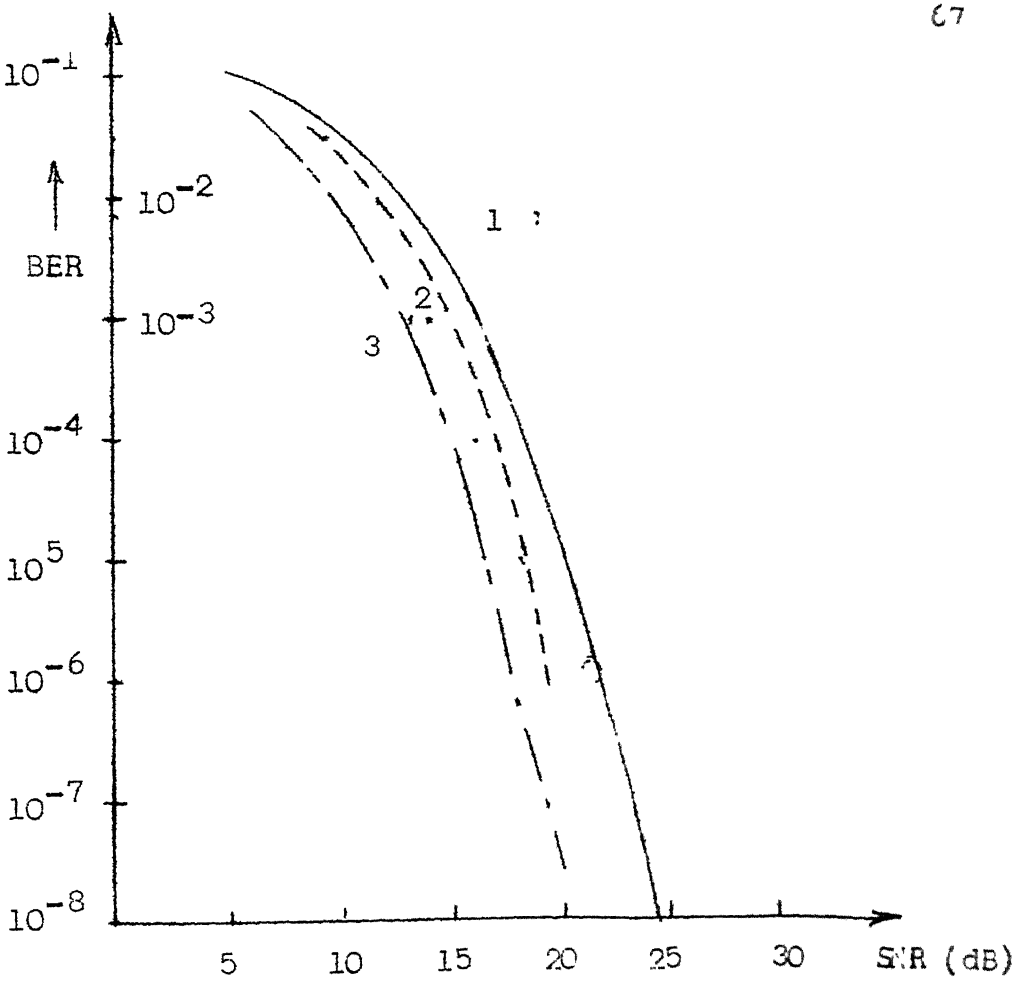
Figure 4.3: SNR degradation test-setup

noise generator (General Radio Company,1390B) with 500 KHz noise bandwidth. The noise was introduced at the input amplifier (733) of the data regenerator. IC733 being a differential amplifier, one input was given the signal and other input was given the noise.

The noise and signal power was measured independently by switching off one of them at a time using the RMS voltmeter (HP 400D). The BER measurements and the SNR measurements were made at various noise levels without changing the signal level. Number of measurements were taken and results averaged. The obtained results are shown in Fig. 4.4 and Table 4.1 alongwith the results given in [10] for comparison. Fig. 4.4 also shows the results without the LPF at the output of the transmitter.

Table 4.1: SNR vs BER Results

SNR	BER
7 dB	4.4×10^{-1}
13 dB	4.7×10^{-2}
16 dB	6.2×10^{-3}
22 dB	5.2×10^{-6}
25.2 dB	2.7×10^{-8}



1) obtained results with LPF
2) results quoted from [10]
3) obtained results without LPF

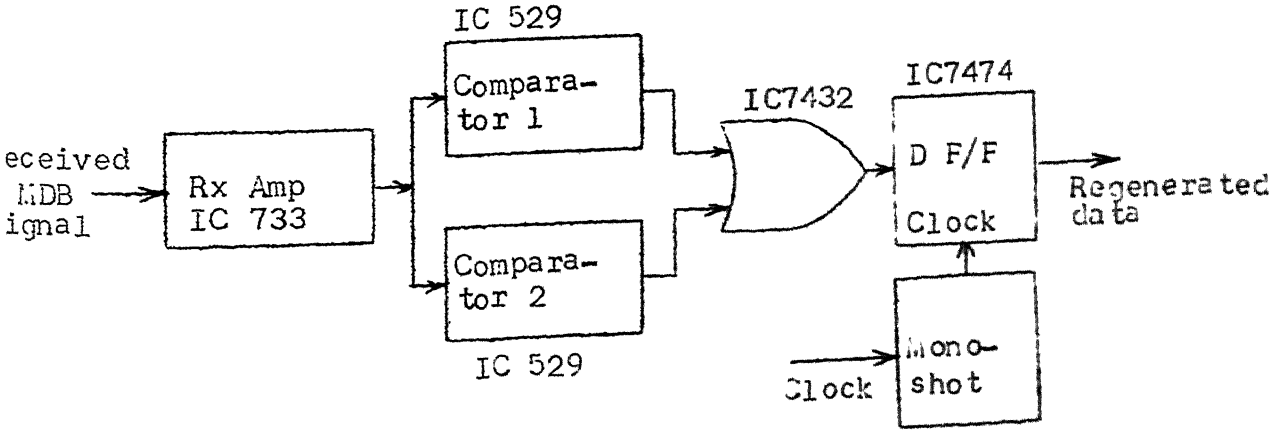
Figure 4.4: SNR vs. Error Rate

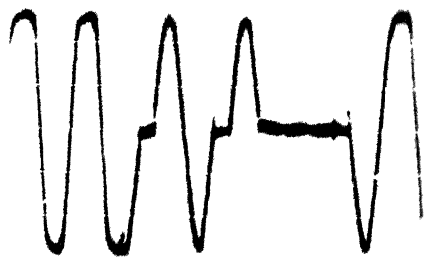
Thus the overall performance of the system was found to be quite satisfactory in terms of BER, eye opening and spectral shaping. The data regenerator shown in Fig. 4.3 is the simple comparator arrangement explained in the next section.

4.5.1 Data Regenerator:

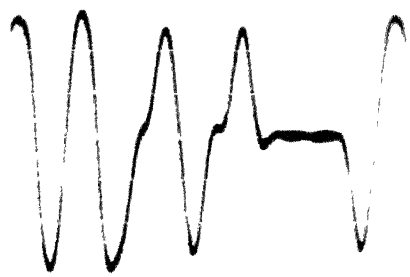
As explained in Chapter 3, the MDB signal has both peak levels representing say a logical one and mid level indicating logical zero. The received MDB signal is amplified and then both extreme levels detected using two comparators. Both comparator outputs are combined and O/P reshaped using clock.

The comparator reference levels are set at half way between the midlevel and the extreme levels and the triggering clock is adjusted in phase to ensure that the sampling is done at centre of the eye. Fig. 4.5 shows the data regenerator block diagram, and the schematic diagram is attached as Appendix E.

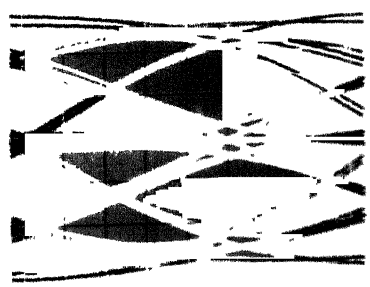




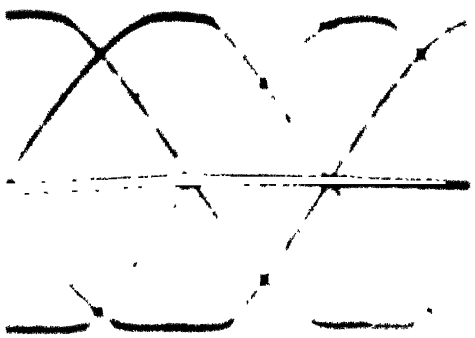
Photograph 1: MDB Waveform (without LPF)



Photograph 2: MDB Waveform (with LPF)

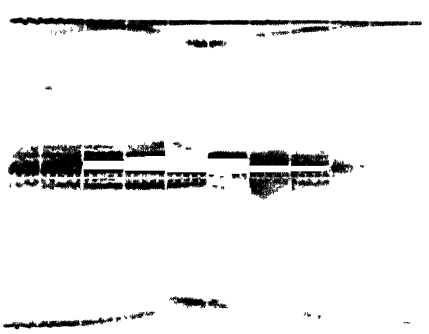


Photograph 3: Eye pattern (with LPF)



Photograph 4: MDB Eye pattern (without LPF)

Photograph 5: Frequency spectrum (MDB)



Photograph 6: Eye pattern (with noise).

CHAPTER 5

CONCLUSION

In the present work the partial response signalling has been implemented using nonlinear waveshaping methods. The use of Gilbert cell for achieving MDB signalling was shown and has been implemented. The data regenerator for the MDB was designed and used for the BER measurements. It was shown in Section 3.5 that the method can be extended to any other PRS polynomial.

In the present work the data rate used was 500 KHz. However the Gilbert cell configuration is capable of much higher switching speeds particularly with emitter degeneration resistances.

The performance of the MDB implementation was tested as given in Chapter 4 and it is seen that the scheme works well in terms of eye openings, out of band spectral power, speed tolerance and bit error rate in the presence of noise. The out of band power and speed tolerance results matched well with the figures available in the literature [3,7,8].

The BER measurements were done using the error detector HP 3761 and by adding noise to the transmitted MDB output. The BER of less than 10^{-9} in the absence of noise (SNR > 25 dB) and of 10^{-2} at SNR = 12 dB were recorded.

5.1 SUGGESTIONS FOR FURTHER WORK:

The following areas are suggested for further work.

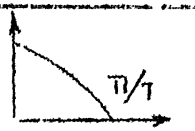
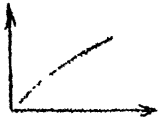
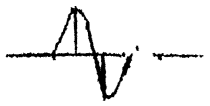
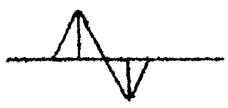
a) Implementation of other system polynomials and polybinary signals using non-linear waveshaping methods.

b) The MDB using waveshaping can be used in applications like packet radio to modulate carrier waves.

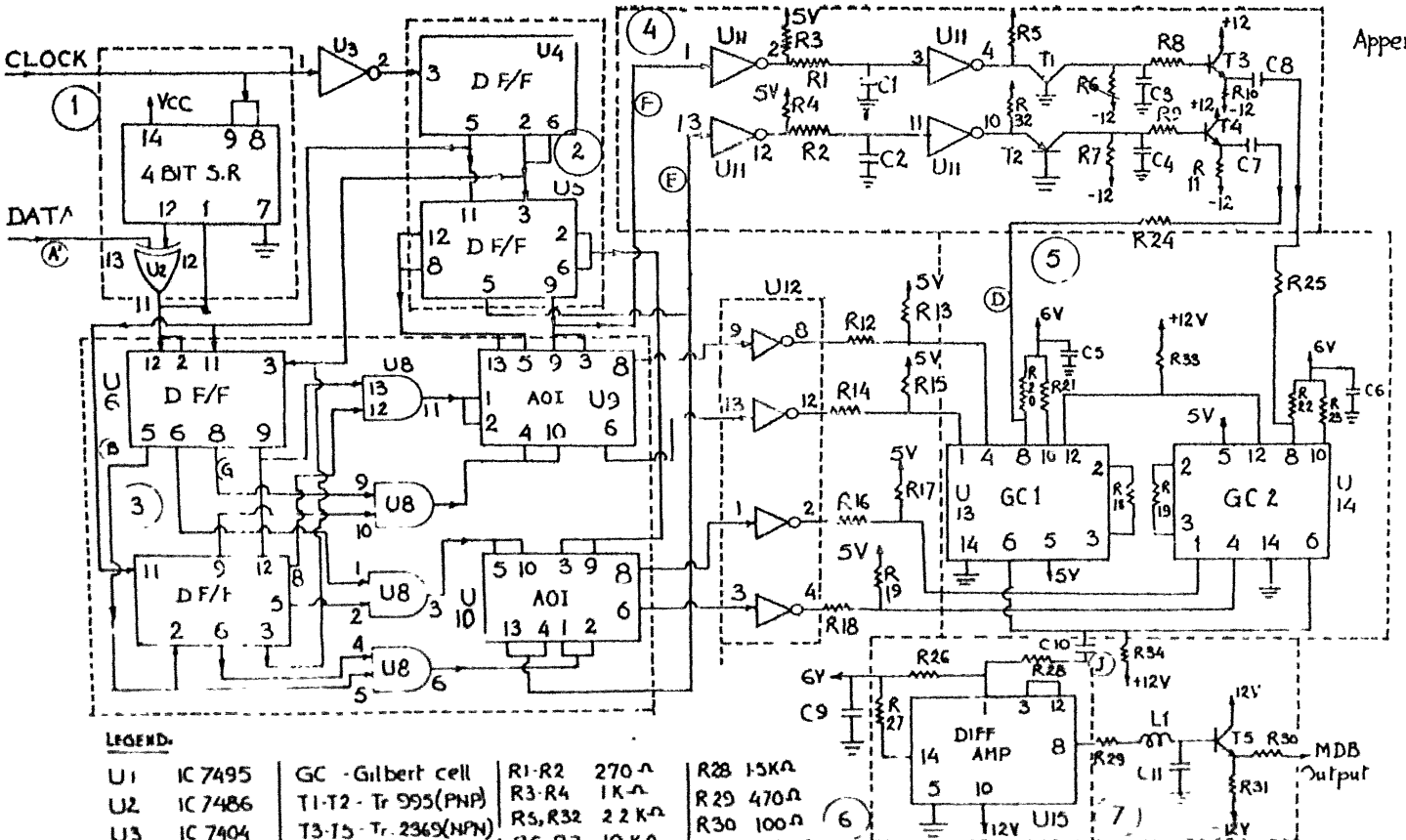
c) The problem of clock recovery has not been covered in this thesis. The same may be carried out based on the methods suggested in the literature [11,12].

d) The degradation due to the LPF in the BER performance is clear from Fig. 4.4. With properly designed low pass filter the performance can be improved.

APPENDIX A

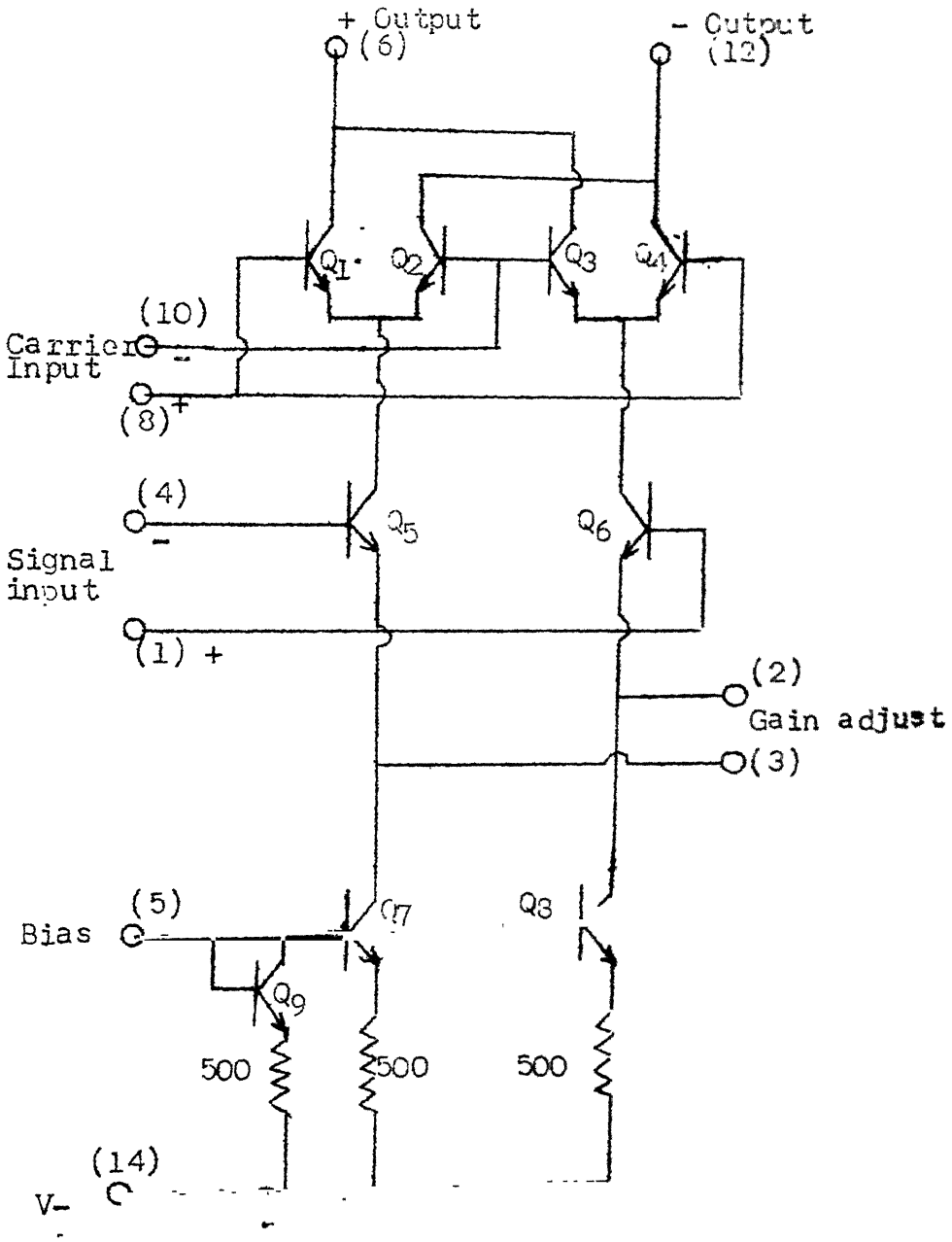
	$\lvert H(\omega)\rvert$	$h(t)$	$\lvert H(\omega)\rvert$ for $\lvert\omega\rvert \leq \pi/T$	Impulse response $h(t)$	Speed tolerance	Min. eye width	No. of O/P levels
ary)			$2T\cos\omega/2T$	$\frac{4T^2}{\pi}\frac{\cos(\pi t/T)}{T^2-4t^2}$	42.5	0.667T	2m-1
			$j2T\sin\frac{\omega}{2}T$	$\frac{8Tt}{\pi}\frac{\cos(\pi t/T)}{4t^2-T^2}$	-	-	2m-1
-D)			$j2T\sin\omega T$	$\frac{2T^2}{\pi}\frac{\sin(\pi t/T)}{t^2-T^2}$	15.5	0.357T	2m-1
2			$4T\cos^2\frac{\omega}{2}T$	$\frac{2T^2}{\pi t}\frac{\sin(\pi t/T)}{T^2-t^2}$	26.6	0.689T	4m-3

Various Partial Response Signalling Schemes



Schematic diagram - MDB transmitter.

APPENDIX C



Schematic Diagram - LM1496 Balanced Mod/Demod.

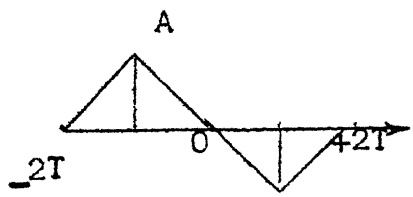
APPENDIX D

CALCULATIONS TO FIND THE EFFECT OF HEIGHT OF TRAPEZOID ON SPECTRAL SHAPING

We consider three types of wave forms i.e. triangle, truncated triangle (trapezoid) and rectangle, All these are normalized in height to contain equal energy.

The Fourier transforms of the three shapes then gives the spectral content of the MDB waveform.

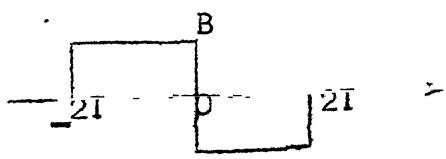
a) Triangle:



$$X(f) = 2AT \frac{\sin^2 \pi fT}{(\pi fT)^2} \times \sin(2\pi fT)$$

where $A = \sqrt{(3/T)}$

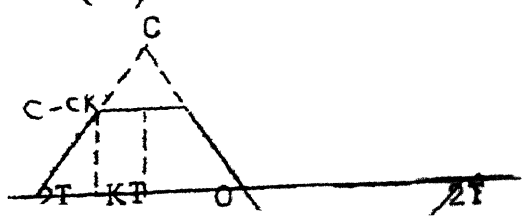
b) Rectangle:



$$X(f) = 4 \cdot BT \cdot \frac{\sin^2(2\pi fT)}{(2\pi fT)}$$

where $B = \sqrt{(1/T)}$

c) Trapezoid:



$$X(f) = (CT\ \mathrm{sinc}^2 \pi fT - (CK)\ KT\ \mathrm{sinc}^2 \pi fKT) \times 2 \sin(2\pi fT)$$

where,

$$C = \left[\frac{3}{T(1-K)^3 + 3KT(1-K)^2} \right]^{1/2}$$

The frequency components at various frequencies were then found using these equations. The results are shown in Figure 3.15. The Gilbert cell used with the emitter degeneration preserves the linearity of the transfer characteristics in which case the side lobes will be [illegible] compared to these results but without the emitter degeneration, the results found above tally with the actual results which can be observed using spectrum analyzer.

-12V
5V
12V
U1
U2
U3
C1
C2
R1
R2
R3
R6
MDS
SIGNAL
BIAS
6V

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